Leading-Edge Memory Solutions

for UltraScale & UltraScale+ FPGAs

(SigmaQuad-II+/SigmaDDR-II+)

GSI Technology customers now have access to a free Controller IP for our SigmaQuad-II+™ and SigmaDDR-II+™ SRAMs, for use with Xilinx UltraScale™ and UltraScale+™ FPGAs.

GSI's SRAM Port IP supports both Burst of 2 (B2) and Burst of 4 (B4) versions of these devices, as well as x18 and x36 data widths.

Multiple Density Support

Quad B2 (x18 & x36)—Up to 500 MHz				
288Mb	144Mb	72Mb	36Mb	18Mb
GS82582Qxx	GS81302QxxA	GS8662QxxB	GS8342QxxB	n/a
Quad B4 (x18 & x36)—Up to 633 MHz				
288Mb	144Mb	72Mb	36Mb	18Mb
GS82582Dxx	GS81302DxxA	GS8662DxxB	GS8342DxxB	GS8182DxxB
DDR B2 (x18 & x36)—Up to 633 MHz				
288Mb	144Mb	72Mb	36Mb	18Mb
GS82582Txx	GS81302TxxA	GS8662TxxB	GS8342TxxB	GS8182TxxB

Controller IP Overview

- Utilizes a "2:1 Mux" configuration for max performance: SRAM clock = 2x FPGA User Interface clock
- Read Latency = ~9 FPGA User Interface clock cycles (2:1 Mux)
- Validated by GSI on a KU040 evaluation board
- Verified by multiple customers with various FPGAs from the UltraScale family

Questions?

Features/Downloads/Documentation:
apps@gsitechnology.com

IP Installation/Timing/Debug:
apps@gsitechnology.com

Engagement Process

- **Review, or assist in creating, customer FPGA —> SRAM pinout**
- **Provide IP source code for simulation**, along with SRAM behavior model**
- **Provide IP source code for synthesis**/P&R/FPGA build**

(Note: IP source code is typically the same for simulation and for synthesis.)**

Available Deliverables

- **Controller IP Source Code (unencrypted Verilog)**
- **Design Constraints File**
- **Controller IP User Guide**
- **SRAM Behavioral Models, for simulation**

Questions?

- **Contact: apps@gsitechnology.com**