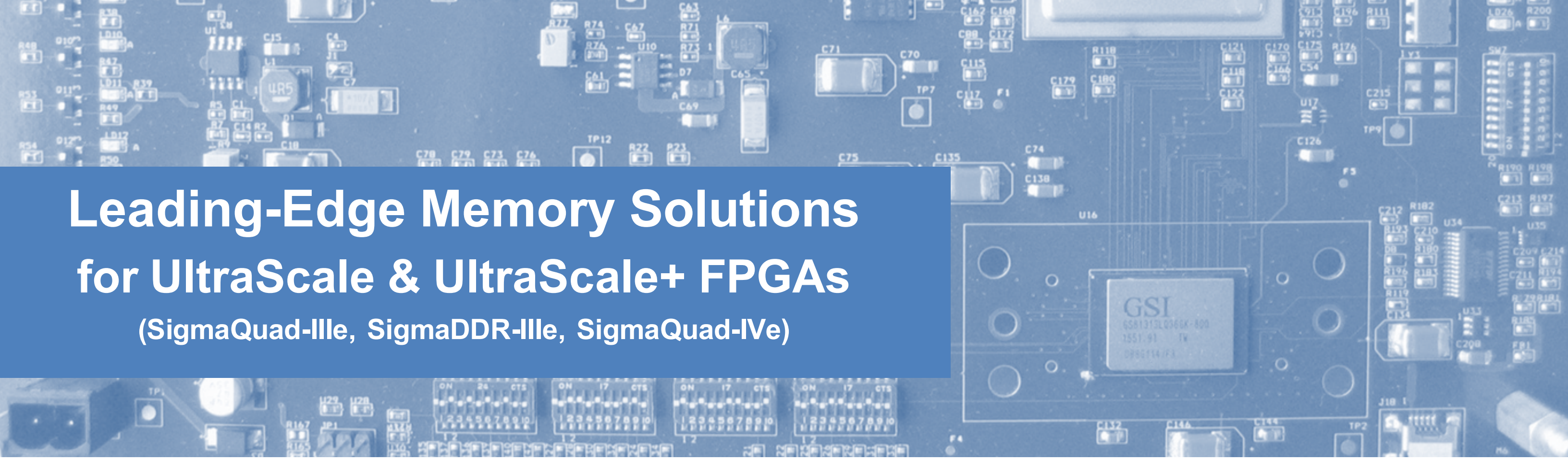

# Leading-Edge Memory Solutions for UltraScale & UltraScale+ FPGAs

(SigmaQuad-IIIe, SigmaDDR-IIIe, SigmaQuad-IVe)

**GSI Technology customers have access to free Controller IP for our SigmaQuad-IIIe™, SigmaDDR-IIIe™, and SigmaQuad-IVe™ SRAMs, for use with AMD/Xilinx UltraScale™ and UltraScale+™ FPGAs.**

## Turbocharge Your Memory Transaction Rate

- **Burst of 2 (B2) and Burst of 4 (B4), x18 and x36 SRAM configurations are supported**
- **No bank/address restrictions up to 933 MHz—eliminates the need for complicated re-order buffers**

## Save Power, Pins, and Board Space vs. Competing Solutions

- **Significantly lower power consumption at equivalent clock frequencies**
- **Fewer clock signals required—helps optimize FPGA I/O bank usage**
- **14 mm x 22 mm, 260-pin BGA SRAM packaging**

| Example Solutions | | Memory Performance | | | |
|---|---|---|---|---|---|
| FPGA | SRAM | Clock Speed | Read Latency | R/W Rate (max) | Data BW (x36, peak) |
| KU040 | 144Mb SQ-IIIe Quad B2 | 800 MHz | 3 cycles | 1.60 GT/s | 115 Gb/s |
| | 144Mb SQ-IIIe Quad B4 | 833 MHz | 3 cycles | 0.86 GT/s | 120 Gb/s |
| KU15P | 144Mb SQ-IVe Quad B2 | 933 MHz | 5 cycles | 1.86 GT/s | 134 Gb/s |
| | 144Mb SQ-IVe Quad B4 | 933 MHz | 5 cycles | 0.93 GT/s | 134 Gb/s |

**Note:** The FPGAs listed are the specific versions GSI used for validating the IP on its evaluation boards.

## Controller IP Overview

- **Utilizes a "4:1 Mux" configuration for max performance: SRAM clock = 4x FPGA User Interface clock; "2:1 Mux" configuration is also available for slower speeds**
- **Read Latency = ~9 FPGA User Interface clock cycles (4:1 Mux)**

D0121; Rev1.0; 10/2025

## Engagement Process

- **Review, or assist in creating, customer FPGA —> SRAM pinout**
- **Provide IP source code for simulation**, along with RAM behavior model**
- **Provide IP source code for synthesis**/P&R/FPGA build**

**(**Note: IP source code is typically the same for simulation and for synthesis.)**

## Available Deliverables

- **Controller IP Source Code (unencrypted Verilog)**
- **Design Constraints File**
- **Controller IP User Guide**
- **SRAM Behavioral Models, for simulation**

## Questions?

- **Contact: [apps@gsitechnology.com](mailto:apps@gsitechnology.com)**