165-Bump BGA
Commercial Temp
Industrial Temp

288Mb SigmaSIO™ DDR-II Burst of 2 SRAM

400 MHz–250 MHz
1.8 V V_{DD}
1.8 V and 1.5 V I/O

Features

- Simultaneous Read and Write SigmaSIO™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- DLL circuitry for wide output data valid window and future frequency scaling
- Burst of 2 Read and Write
- 1.8 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- RoHS-compliant 165-bump BGA package

SigmaSIO™ Family Overview

GS82582S18/36GE are built in compliance with the SigmaSIO DDR-II SRAM pinout standard for Separate I/O synchronous SRAMs. They are 301,989,888-bit (288Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

Clocking and Addressing Schemes

A Burst of 2 SigmaSIO DDR-II SRAM is a synchronous device. It employs dual input register clock inputs, K and $\overline{K}$. The device also allows the user to manipulate the output register clock input quasi independently with dual output register clock inputs, C and $\overline{C}$. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead. Each Burst of 2 SigmaSIO DDR-II SRAM also supplies Echo Clock outputs, CQ and $\overline{CQ}$, which are synchronized with read data output. When used in a source synchronous clocking scheme, the Echo Clock outputs can be used to fire input registers at the data's destination.

Each internal read and write operation in a SigmaSIO DDR-II B2 RAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaSIO DDR-II B2 is always one address pin less than the advertised index depth (e.g., the 16M x 18 has an 8M addressable index).

Parameter Synopsis

	-400	-375	-333	-300	-250
tKHKH	2.5 ns	2.66 ns	3.0 ns	3.3 ns	4.0 ns
tKHQV	0.45 ns	0.45 ns	0.45 ns	0.45 ns	0.45 ns

16M x 18 SigmaQuad SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW1}$	$\overline{K}$	SA	$\overline{LD}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{D}_{\overline{OFF}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.
2. A7 is the expansion address.

8M x 36 SigmaQuad SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	R/$\overline{\text{W}}$	$\overline{\text{BW2}}$	$\overline{\text{K}}$	$\overline{\text{BW1}}$	$\overline{\text{LD}}$	SA	SA	CQ
B	Q27	Q18	D18	SA	$\overline{\text{BW3}}$	K	$\overline{\text{BW0}}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{\text{D}}_{\overline{\text{OFF}}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{\text{BW0}}$ controls writes to D0:D8. $\overline{\text{BW1}}$ controls writes to D9:D17.
2. $\overline{\text{BW2}}$ controls writes to D18:D26. $\overline{\text{BW3}}$ controls writes to D27:D35.
3. A2 is the expansion address.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
R/$\overline{W}$	Read/Write Contol Pin	Input	Write Active Low; Read Active High
$\overline{BW0}$–$\overline{BW1}$	Synchronous Byte Writes	Input	Active Low x18 Version
$\overline{BW0}$–$\overline{BW3}$	Synchronous Byte Writes	Input	Active Low x36 Version
K	Input Clock	Input	Active High
C	Output Clock	Input	Active High
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
$\overline{K}$	Input Clock	Input	Active Low
$\overline{C}$	Output Clock	Output	Active Low
$\overline{D_{OFF}}$	DLL Disable	—	Active Low
$\overline{LD}$	Synchronous Load Pin	—	Active Low
$\overline{CQ}$	Output Echo Clock	Output	Active Low
CQ	Output Echo Clock	Output	Active High
Dn	Synchronous Data Inputs	Input	—
Qn	Synchronous Data Outputs	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
NC	No Connect	—	—

Notes:
1. C, $\overline{C}$, K, or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DDQ}, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. NC = Not Connected to die or any other pin

Background

Separate I/O SRAMs, like SigmaQuad SRAMs, are attractive in applications where alternating reads and writes are needed. On the other hand, Common I/O SRAMs like the SigmaCIO family are popular in applications where bursts of read or write traffic are needed. The SigmaSIO SRAM is a hybrid of these two devices. Like the SigmaQuad family devices, the SigmaSIO features a separate I/O data path, offering the user independent Data In and Data Out pins. However, the SigmaSIO devices offer a control protocol like that offered on the SigmaCIO devices. Therefore, while SigmaQuad SRAMs allow a user to operate both data ports at the same time, they force alternating loads of read and write addresses. SigmaSIO SRAMs allow continuous loads of read or write addresses like SigmaCIO SRAMs, but in a separate I/O configuration.

Like a SigmaQuad SRAM, a SigmaSIO DDR-II SRAM can execute an alternating sequence of reads and writes. However, doing so results in the Data In port and the Data Out port stalling with nothing to do on alternate transfers. A SigmaQuad device would keep both ports running at capacity full time. On the other hand, the SigmaSIO device can accept a continuous stream of read commands and read data or a continuous stream of write commands and write data. The SigmaQuad device, by contrast, restricts the user from loading a continuous stream of read or write addresses. The advantage of the SigmaSIO device is that it allows twice the random address bandwidth for either reads or writes than could be acheived with a SigmaQuad version of the device. SigmaDDR (CIO) SRAMs offer this same advantage, but do not have the separate Data In and Data Out pins offered on the SigmaSIO SRAMs. Therefore, SigmaSIO devices are useful in psuedo dual port SRAM applications where communication of burst traffic between two electrically independent busses is desired.

Each of the three SigmaQuad Family SRAMs—SigmaQuad, SigmaDDR, and SigmaSIO—supports similar address rates because random address rate is determined by the internal performance of the RAM. In addition, all three SigmaQuad Family SRAMs are based on the same internal circuits. Differences between the truth tables of the different devices proceed from differences in how the RAM's interface is contrived to interact with the rest of the system. Each mode of operation has its own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

Burst of 2 SigmaSIO DDR-II SRAM DDR Read

The status of the Address Input, R/$\overline{W}$, and $\overline{LD}$ pins are sampled at each rising edge of K. $\overline{LD}$ high causes chip disable. A high on the R/$\overline{W}$ pin begins a read cycle. The two resulting data output transfers begin after the next rising edge of the K clock. Data is clocked out by the next rising edge of the $\overline{C}$ if it is active. Otherwise, data is clocked out at the next rising edge of $\overline{K}$. The next data chunk is clocked out on the rising edge of C, if active. Otherwise, data is clocked out on the rising edge of K.

Burst of 2 SigmaSIO DDR-II SRAM DDR Write

The status of the Address Input, R/$\overline{W}$, and $\overline{LD}$ pins are sampled at each rising edge of K. $\overline{LD}$ high causes chip disable. A low on the R/$\overline{W}$ pin, begins a write cycle. Data is clocked in by the next rising edge of K and then the rising edge of $\overline{K}$.

Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2-beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

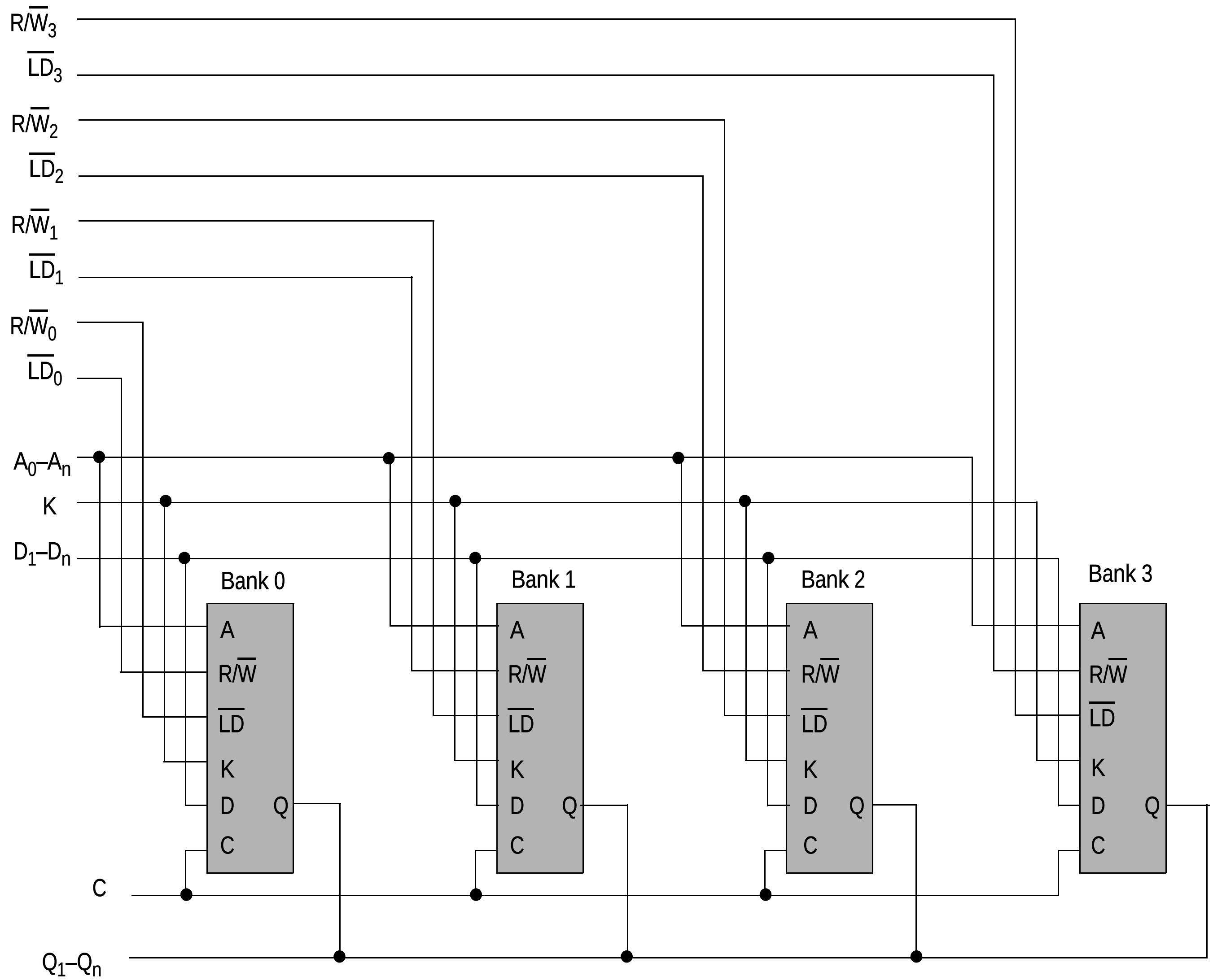
Resulting Write Operation

Beat 1		Beat 2	
D0–D8	D9–D17	D0–D8	D9–D17
Written	Unchanged	Unchanged	Written

Output Register Control

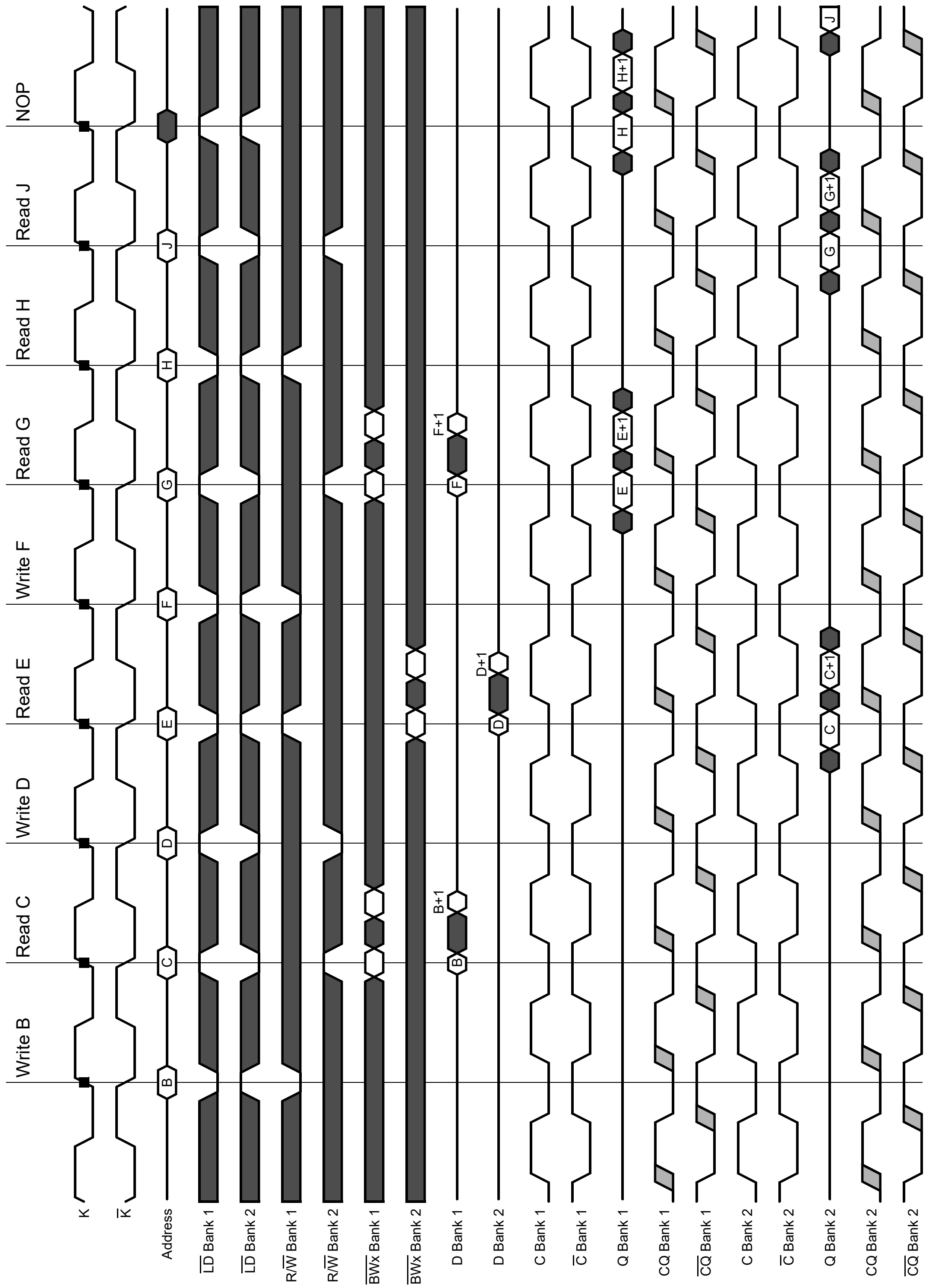
SigmaSIO DDR-II SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and $\overline{C}$. The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and $\overline{K}$ clocks. If the C and $\overline{C}$ clock inputs are tied high, the RAM reverts to K and $\overline{K}$ control of the outputs.

Example Four Bank Depth Expansion Schematic



Note:
For simplicity $\overline{BWn}$ is not shown.

Burst of 2 SigmaSIO DDR-II SRAM Depth Expansion



FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaSIO DDR-II SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a vendor-specified tolerance is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Power-Up Initialization

After power-up, stable input clocks must be applied to the device for 20 µs prior to issuing read and write commands. See the t_{KInit} timing parameter in the **AC Electrical Characteristics** section.

Note:
The t_{KInit} requirement is independent of the tLock requirement, which specifies how many cycles of stable input clocks (2048) must be applied after the $\overline{\text{Doff}}$ pin has been driven High in order to ensure that the DLL locks properly (and the DLL must lock properly before issuing read and write commands). However, t_{KInit} is greater than t_{KLock}, even at the slowest permitted cycle time of 8.4 ns (2048*8.4 ns = 17.2 µs). Consequently, the 20 µs associated with t_{KInit} is sufficient to cover the t_{KLock} requirement at power-up if the $\overline{\text{Doff}}$ pin is driven High prior to the start of the 20 µs period.

Also, t_{KInit} only needs to be met once, immediately after power-up, whereas t_{KLock} must be met any time the DLL is disabled/reset (whether by toggling $\overline{\text{Doff}}$ Low or by stopping K clocks for > 30 ns).

Separate I/O Burst of 2 Sigma SIO-II SRAM Truth Table

A	$\overline{\text{LD}}$	R/$\overline{\text{W}}$	Current Operation	D	D	Q	Q
K↑ (t_n)	K↑ (t_n)	K↑ (t_n)	K↑ (t_n)	K↑ (t_{n+1})	$\overline{\text{K}}$↑ ($t_{n+1½}$)	$\overline{\text{K}}$↑ ($t_{n+1½}$)	K↑ (t_{n+2})
X	1	X	Deselect	X	X	Hi-Z	Hi-Z
V	0	1	Read	X	X	Q0	Q1
V	0	0	Write	D0	D1	Hi-Z	Hi-Z

Notes:
1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care"
2. Q0 and Q1 indicate the first and second pieces of output data transferred during Read operations.
3. D0 and D1 indicate the first and second pieces of input data transferred during Write operations.
4. Users should not clock in metastable addresses.

B2 Byte Write Clock Truth Table

$\overline{BW}$	$\overline{BW}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{BWn}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = "T", else $\overline{BW}$ = "F".

x36 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$	$\overline{BW0}$	D27–D35	D18–D26	D9–D17	D0–D8
1	1	1	1	Don’t Care	Don’t Care	Don’t Care	Don’t Care
0	1	1	1	Don’t Care	Don’t Care	Don’t Care	Data In
1	0	1	1	Don’t Care	Don’t Care	Data In	Don’t Care
0	0	1	1	Don’t Care	Don’t Care	Data In	Data In
1	1	0	1	Don’t Care	Data In	Don’t Care	Don’t Care
0	1	0	1	Don’t Care	Data In	Don’t Care	Data In
1	0	0	1	Don’t Care	Data In	Data In	Don’t Care
0	0	0	1	Don’t Care	Data In	Data In	Data In
1	1	1	0	Data In	Don’t Care	Don’t Care	Don’t Care
0	1	1	0	Data In	Don’t Care	Don’t Care	Data In
1	0	1	0	Data In	Don’t Care	Data In	Don’t Care
0	0	1	0	Data In	Don’t Care	Data In	Data In
1	1	0	0	Data In	Data In	Don’t Care	Don’t Care
0	1	0	0	Data In	Data In	Don’t Care	Data In
1	0	0	0	Data In	Data In	Data In	Don’t Care
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don’t Care	Don’t Care
0	1	Data In	Don’t Care
1	0	Don’t Care	Data In
0	0	Data In	Data In

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.9	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.3 (≤ 2.9 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.3 (≤ 2.9 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	^oC
T_{STG}	Storage Temperature	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	0.68	—	0.95	V

Note:
The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}. For more information, read AN1021 SigmaQuad and SigmaDDR Power-Up.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

Note:
* The part numbers of Industrial Temperature Range versions end with the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
165 BGA	4-layer	16.10	13.69	12.73	6.54	2.08

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 0.1	V_{DDQ} + 0.3	mV	1
DC Input Logic Low	V_{IL} (dc)	–0.3	V_{REF} – 0.1	mV	1

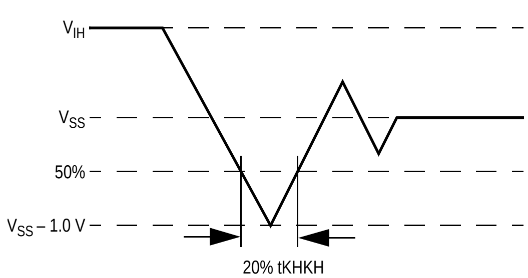
Note:
Compatible with both 1.8 V and 1.5 V I/O drivers

HSTL I/O AC Input Characteristics

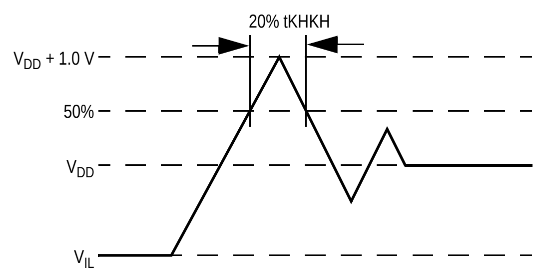
Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 0.2	—	mV	2,3
AC Input Logic Low	V_{IL} (ac)	—	V_{REF} – 0.2	mV	2,3
V_{REF} Peak- to-Peak AC Voltage	V_{REF} (ac)	—	5% V_{REF} (DC)	mV	1

Notes:
1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. To guarantee AC characteristics, V_{IH},V_{IL}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF
Clock Capacitance	C_{CLK}	—	5	6	pF

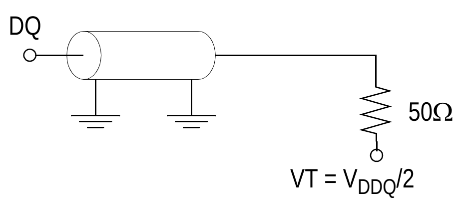
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
V_{REF} = 0.75 V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
$\overline{\text{Doff}}$	$I_{IL\overline{DOFF}}$	V_{IN} = 0 to V_{DD}	–2 uA	100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA

Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2 – 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	V_{OL1}	$V_{DDQ}/2 – 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	V_{OH2}	$V_{DDQ} – 0.2$	V_{DDQ}	V	4, 5
Output Low Voltage	V_{OL2}	Vss	0.2	V	4, 6

Notes:
1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5 V or 1.8 V
4. $0\Omega \leq RQ \leq \infty\Omega$
5. I_{OH} = –1.0 mA
6. I_{OL} = 1.0 mA

Operating Currents

Parameter	Symbol	Test Conditions	-400		-375		-333		-300		-250		Unit	Notes
			0 to 70°C	−40 to 85°C	0 to 70°C	−40 to 85°C	0 to 70°C	−40 to 85°C	0 to 70°C	−40 to 85°C	0 to 70°C	−40 to 85°C		
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	820	840	780	800	700	720	650	670	560	580	mA	2, 3
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	760	780	720	740	660	680	610	630	530	550	mA	2, 3
Standby Current (NOP): DDR	I_{SB1}	Device deselected, I^{OUT} = 0 mA, f = Max, All Inputs ≤ 0.2 V or ≥ V_{DD} – 0.2 V	470	490	450	470	420	440	400	420	360	380	mA	2, 4

Notes:
1. Power measured with output pins floating.
2. Minimum cycle, I_{OUT} = 0 mA
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.

AC Electrical Characteristics

Parameter	Symbol	-400		-375		-333		-300		-250		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock													
K, $\overline{K}$ Clock Cycle Time C, C Clock Cycle Time	t_{KHKH} t_{CHCH}	2.5	8.4	2.66	8.4	3.0	4.5	3.3	4.5	4.0	8.4	ns	
tKC Variable	t_{KCVar}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	6
K, $\overline{K}$ Clock High Pulse Width C, C Clock High Pulse Width	t_{KHKL} t_{CHCL}	1.0	—	1.06	—	1.2	—	1.32	—	1.6	—	ns	
K, $\overline{K}$ Clock Low Pulse Width C, C Clock Low Pulse Width	t_{KLKH} t_{CLCH}	1.0	—	1.06	—	1.2	—	1.32	—	1.6	—	ns	
K to $\overline{K}$ High C to C High	$t_{KH\overline{K}H}$ $t_{CH\overline{C}H}$	1.5	—	1.13	—	1.35	—	1.49	—	1.8	—	ns	
$\overline{K}$ to K High C to C High	$t_{\overline{K}HKH}$ $t_{\overline{C}HCH}$	1.5	—	1.13	—	1.35	—	1.49	—	1.8	—	ns	
K, $\overline{K}$ Clock High to C, $\overline{C}$ Clock High	t_{KHCH}	0	1.21	0	1.21	0	1.35	0	1.49	0	1.8	ns	
DLL Lock Time	t_{KLock}	1024	—	1024	—	1024	—	1024	—	1024	—	cycle	7
K Static to DLL reset	t_{KReset}	30	—	30	—	30	—	30	—	30	—	ns	
K, $\overline{K}$ Clock Initialization	t_{KInit}	20	—	20	—	20	—	20	—	20	—	μs	9
Output Times													
K, $\overline{K}$ Clock High to Data Output Valid C, C Clock High to Data Output Valid	t_{KHQV} t_{CHQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	4
K, $\overline{K}$ Clock High to Data Output Hold C, C Clock High to Data Output Hold	t_{KHQX} t_{CHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	4
K, $\overline{K}$ Clock High to Echo Clock Valid C, C Clock High to Echo Clock Valid	t_{KHCQV} t_{CHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold C, C Clock High to Echo Clock Hold	t_{KHCQX} t_{CHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	t_{CQHQV}	—	0.2	—	0.2	—	0.25	—	0.27	—	0.30	ns	8
CQ, $\overline{CQ}$ High Output Hold	t_{CQHQX}	–0.2	—	–0.2	—	–0.25	—	–0.27	—	–0.30	—	ns	8
CQ Phase Distortion	$t_{CQH\overline{CQ}H}$ $t_{\overline{CQ}HCQH}$	1.0	—	1.0	—	1.10	—	1.24	—	1.55	—	ns	
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	t_{KHQZ} t_{CHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	4

Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are R/ $\overline{W}$, $\overline{LD}$.
3. Control singles are $\overline{BW0}$, $\overline{BW1}$ (and $\overline{BW2}$, $\overline{BW3}$ for x36).
4. If C, $\overline{C}$ are tied high, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters
5. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two SRAMs on the same board to be at such different voltages and temperatures.
6. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
7. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
8. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.
9. After device power-up, 20μs of stable input clocks (as specified by t_{KInit}) must be supplied before reads and writes are issued.

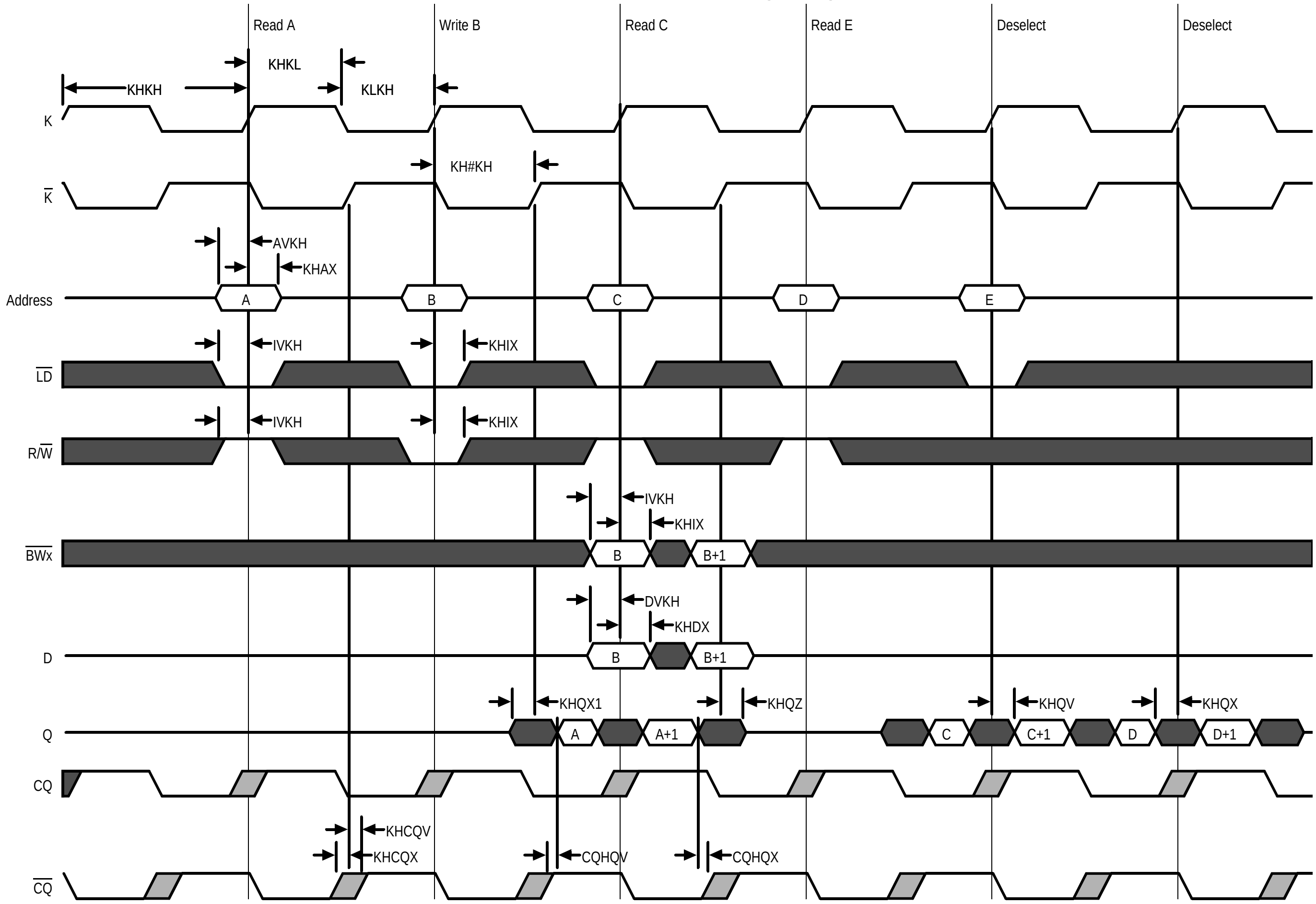
AC Electrical Characteristics (Continued)

Parameter	Symbol	-400		-375		-333		-300		-250		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	t_{KHQX1} t_{CHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	4
Setup Times													
Address Input Setup Time	t_{AVKH}	0.4	—	0.4	—	0.4	—	0.4	—	0.5	—	ns	1
Control Input Setup Time(R/ $\overline{W}$) ($\overline{LD}$)	t_{IVKH}	0.4	—	0.4	—	0.4	—	0.4	—	0.5	—	ns	2
Control Input Setup Time (BWX) (NWX)	t_{IVKH}	0.28	—	0.28	—	0.28	—	0.3	—	0.35	—	ns	3
Data Input Setup Time	t_{DVKH}	0.28	—	0.28	—	0.28	—	0.3	—	0.35	—	ns	
Hold Times													
Address Input Hold Time	t_{KHAX}	0.4	—	0.4	—	0.4	—	0.4	—	0.5	—	ns	1
Control Input Hold Time (R/ $\overline{W}$) ($\overline{LD}$)	t_{KHIX}	0.4	—	0.4	—	0.4	—	0.4	—	0.5	—	ns	2
Control Input Hold Time (BWX) (NWX)	t_{KHIX}	0.28	—	0.28	—	0.28	—	0.3	—	0.35	—	ns	3
Data Input Hold Time	t_{KHDX}	0.28	—	0.28	—	0.28	—	0.3	—	0.35	—	ns	

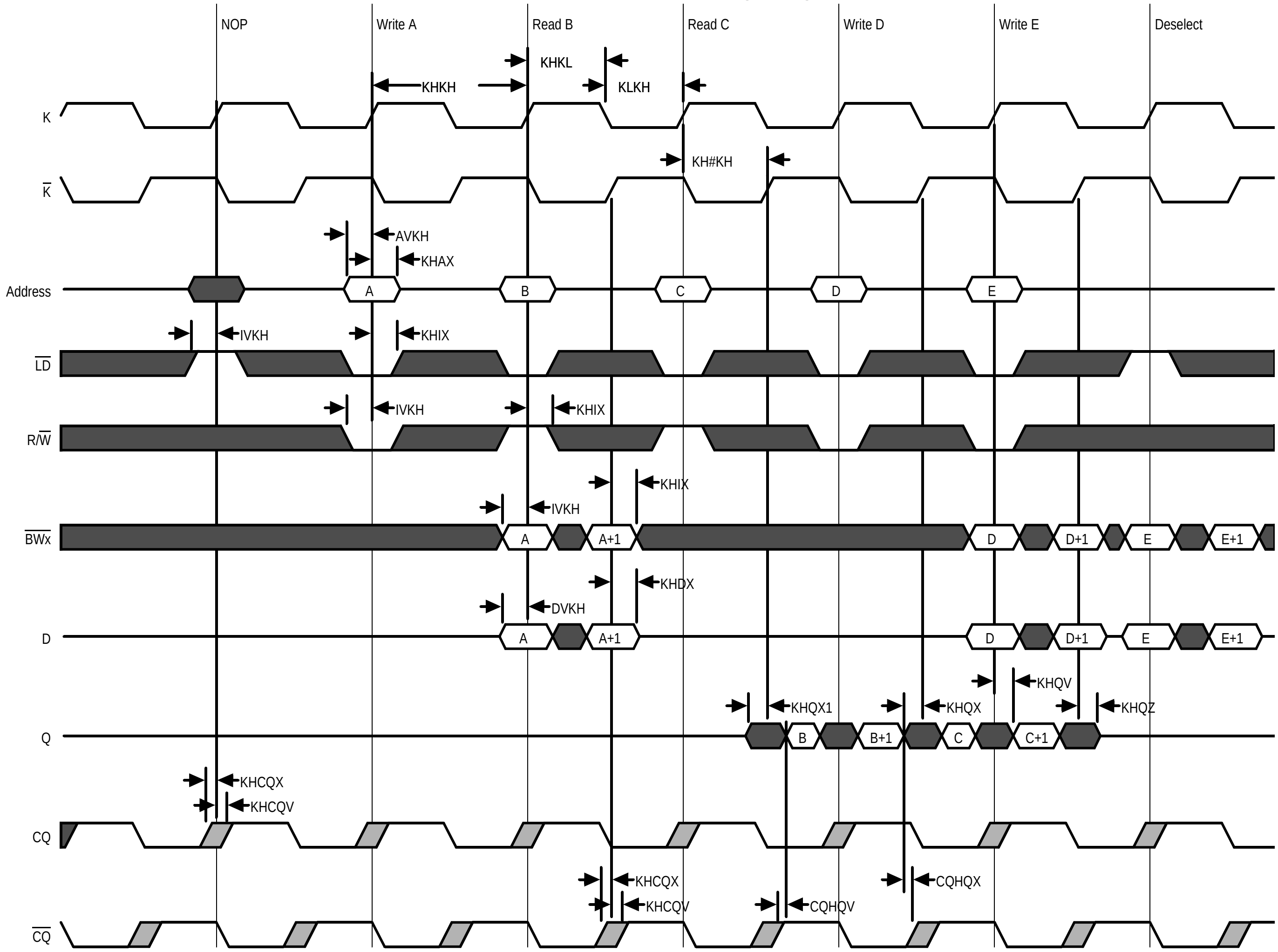
Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are R/ $\overline{W}$, $\overline{LD}$.
3. Control singles are $\overline{BW0}$, $\overline{BW1}$ (and $\overline{BW2}$, $\overline{BW3}$ for x36).
4. If C, $\overline{C}$ are tied high, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters
5. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two SRAMs on the same board to be at such different voltages and temperatures.
6. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
7. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
8. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.
9. After device power-up, 20µs of stable input clocks (as specified by t_{KInit}) must be supplied before reads and writes are issued.

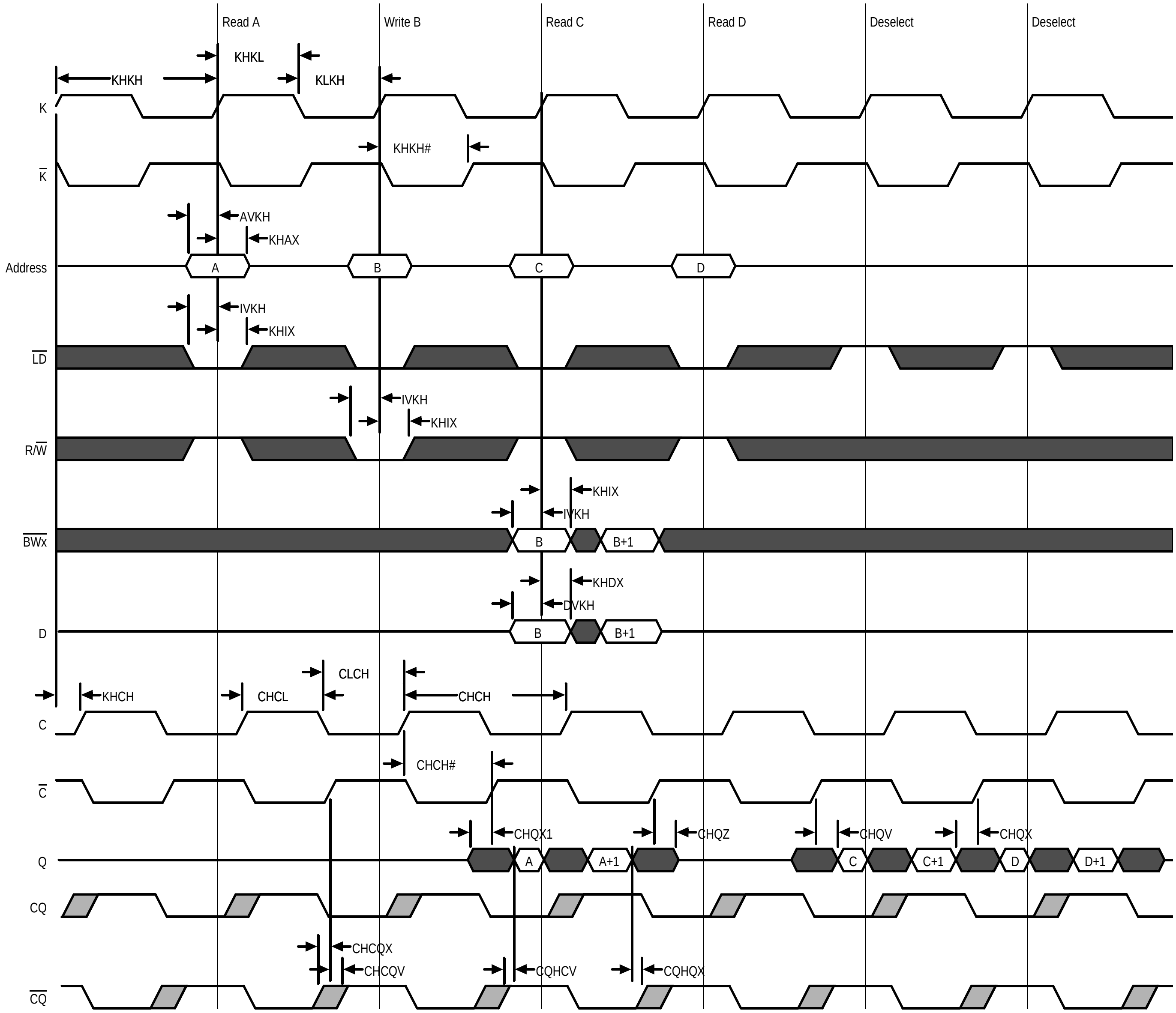
K Controlled Read-First Timing Diagram



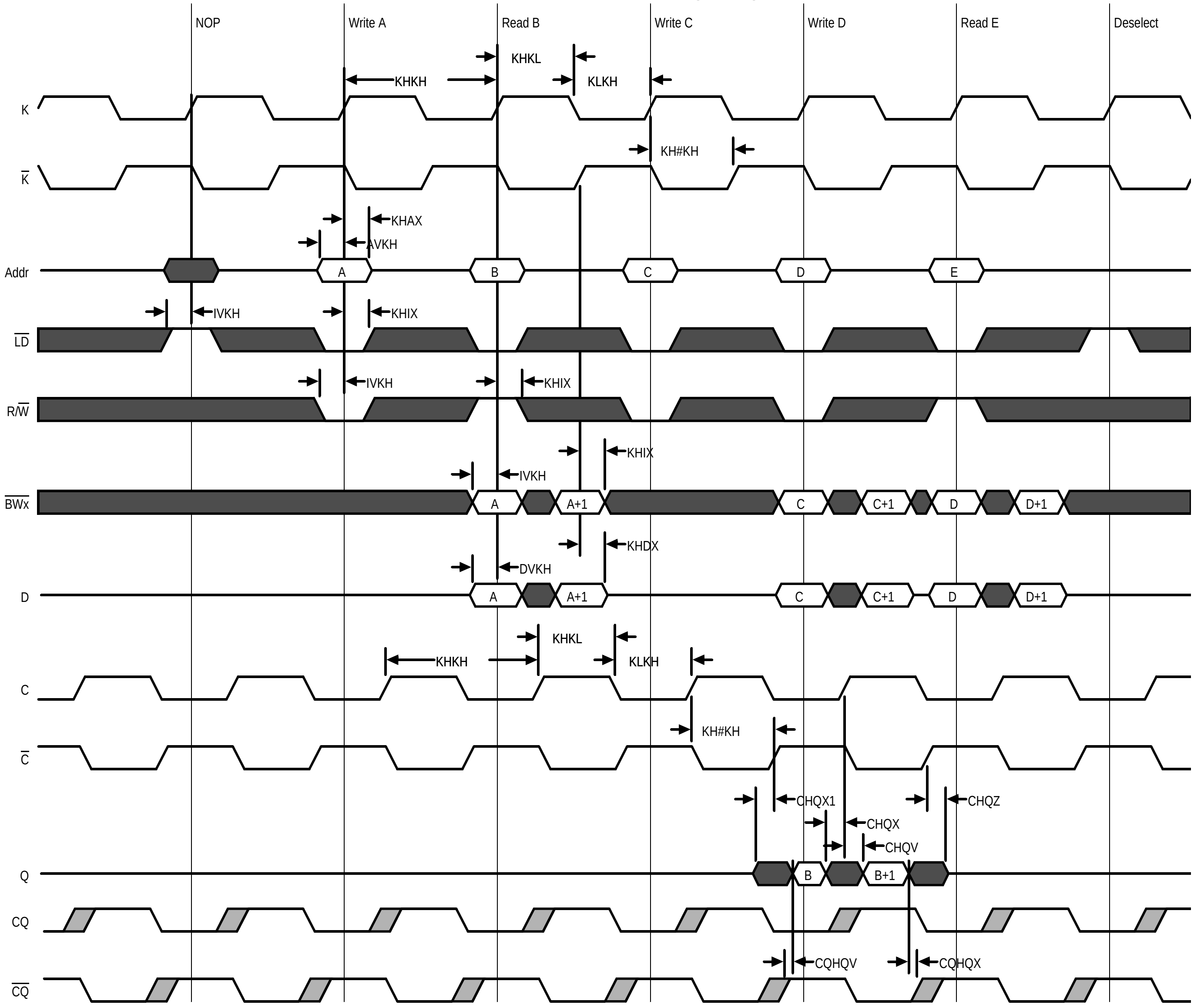
K Controlled Write-First Timing Diagram



C Controlled Read-First Timing Diagram



C Controlled Write-First Timing Diagram



JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DD}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

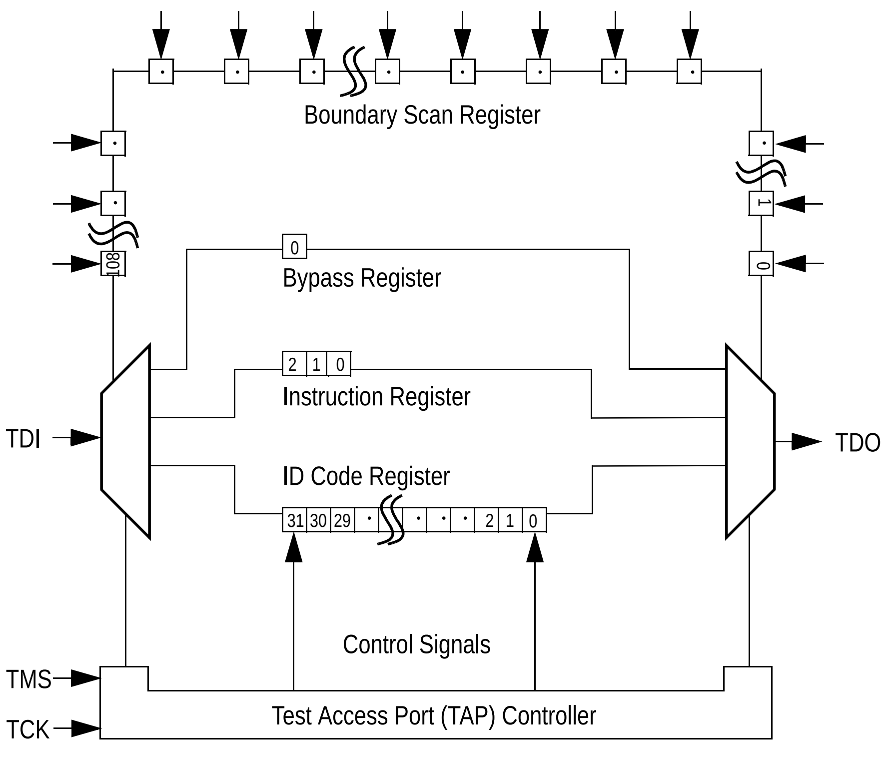
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM’s JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	See BSDL Model																				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

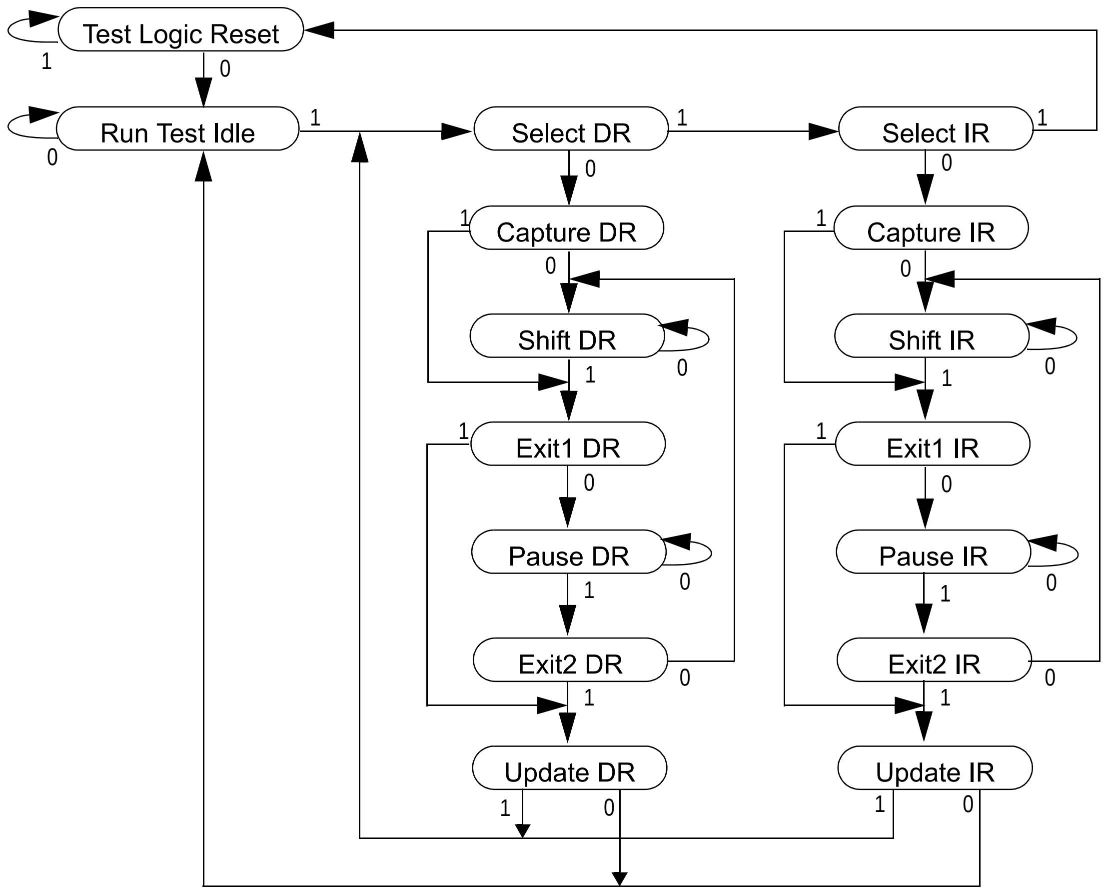
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
GSI	011	GSI private instruction.	1
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
GSI	110	GSI private instruction.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input Low Voltage	V_{ILJ}	–0.3	0.3 * V_{DD}	V	1
Test Port Input High Voltage	V_{IHJ}	0.7 * V_{DD}	V_{DD} +0.3	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	V_{DD} – 0.2	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.2	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DD} – 0.1	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	0.1	V	5, 9

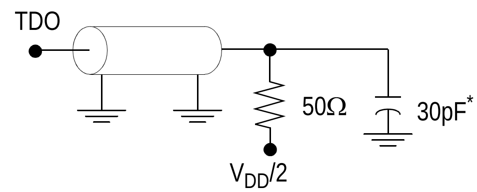
Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < V_{DDn} +1 V not to exceed 2.9 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \le V_{IN} \le V_{DDn}$
3. $0 V \le V_{IN} \le V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DD} supply.
6. I_{OHJ} = –2 mA
7. I_{OLJ} = + 2 mA
8. I_{OHJC} = –100 uA
9. I_{OLJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DD}/2

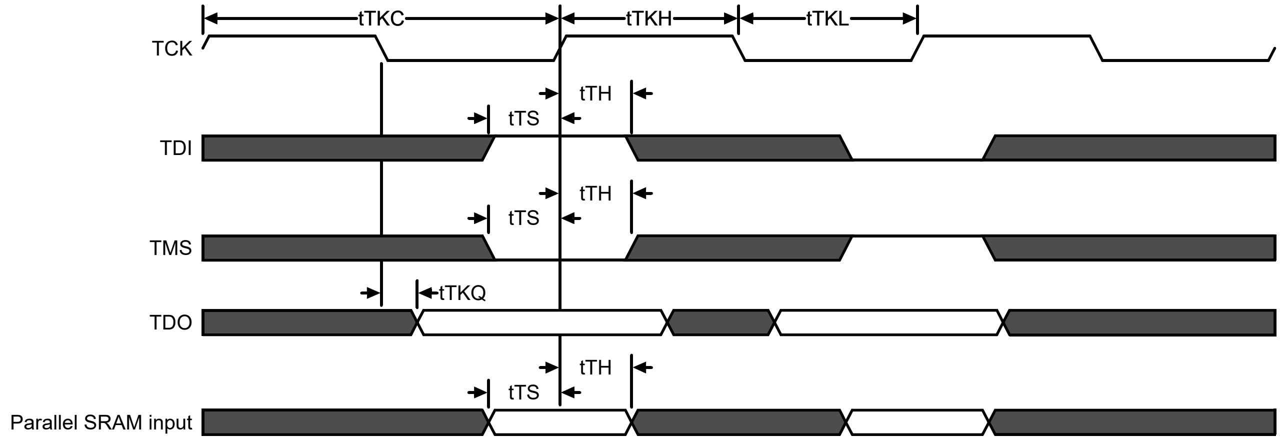
Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

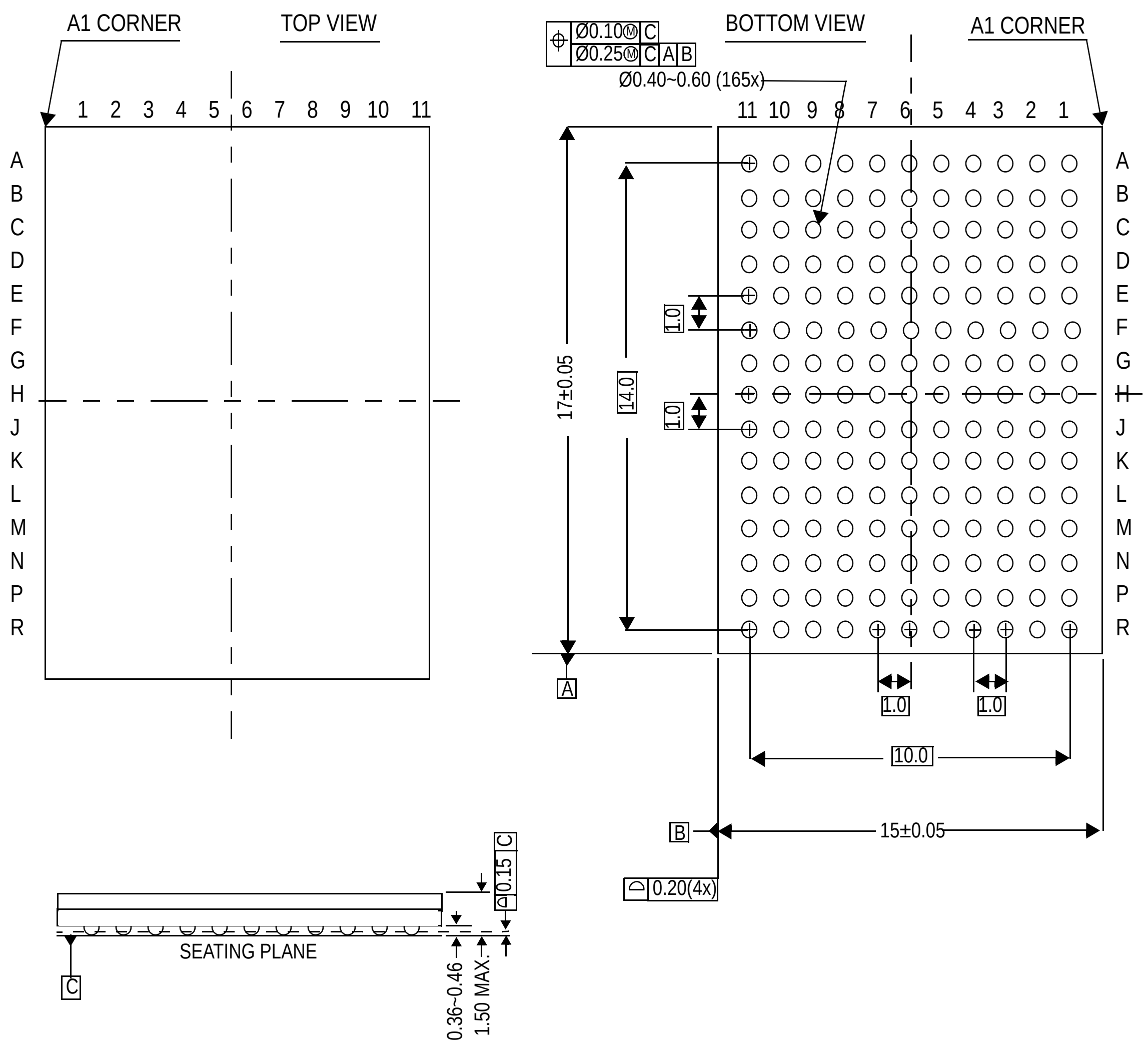
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Package Dimensions—165-Bump FPBGA (Package GE)



Ordering Information—GSI SigmaSIO DDR-II SRAM

Org	Part Number1	Type	Package	Speed (MHz)	T_J[2]
16M x 18	GS82582S18GE-400	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	400	C
16M x 18	GS82582S18GE-375	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	375	C
16M x 18	GS82582S18GE-333	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	333	C
16M x 18	GS82582S18GE-300	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	300	C
16M x 18	GS82582S18GE-250	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	250	C
16M x 18	GS82582S18GE-400I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	400	I
16M x 18	GS82582S18GE-375I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	375	I
16M x 18	GS82582S18GE-333I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	333	I
16M x 18	GS82582S18GE-300I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	300	I
16M x 18	GS82582S18GE-250I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	250	I
8M x 36	GS82582S36GE-400	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	400	C
8M x 36	GS82582S36GE-375	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	375	C
8M x 36	GS82582S36GE-333	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	333	C
8M x 36	GS82582S36GE-300	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	300	C
8M x 36	GS82582S36GE-250	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	250	C
8M x 36	GS82582S36GE-400I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	400	I
8M x 36	GS82582S36GE-375I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	375	I
8M x 36	GS82582S36GE-333I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	333	I
8M x 36	GS82582S36GE-300I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	300	I
8M x 36	GS82582S36GE-250I	SigmaSIO DDR-II SRAM	RoHS-compliant 165-bump BGA	250	I

Notes:

1. For Tape and Reel add the character “T” to the end of the part number. Example: GS82582S36GE-300T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

SigmaSIO DDR-II Revision History

File Name	Format/Content	Description of changes
82582Sxx_r1		Creation of datasheet
82582Sxx_r1_01	Content	Updated speed bin offerings
82582Sxx_r1_02	Content	Removed x8 and x9 configurations
82582Sxx_r1_03	Content	• Removed leaded part numbers • Added Power-Up Initialization section on page 10 • Added tKInit specification
82582Sxx_r1_04	Content	• Removed Preliminary banner • Added Op Current CZ data • (Rev1.04a: Corrected erroneous information in Input and Output Leakage Characteristics table)

