

**BGA**  
**Commercial Temp**  
**Industrial Temp**

# 512K x 16

## 8Mb Asynchronous SRAM

**8, 10, 12 ns**  
**3.3 V V<sub>DD</sub>**

### Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 240/190/170 mA at minimum cycle time
- Single 3.3 V ± 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- 14 mm x 22 mm, 119-bump, 1.27 mm Pitch Ball Grid Array package
- RoHS-compliant package available

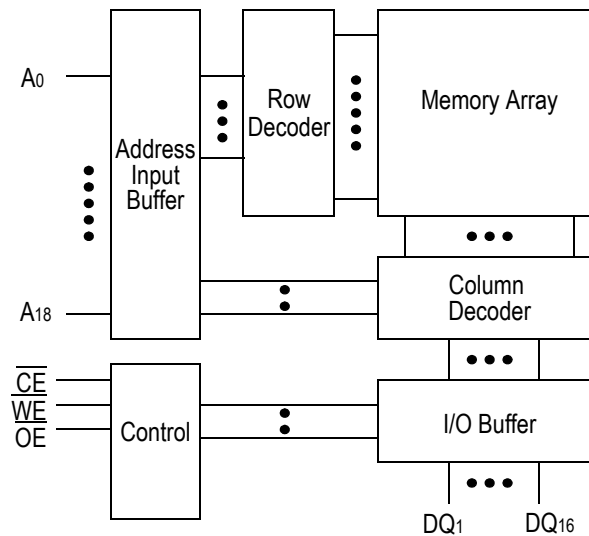
### Description

The GS78116A is a high speed CMOS Static RAM organized as 524,288-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. The GS78116A operates on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS78116 is available in a 14 mm x 22 mm BGA package.

### Pin Descriptions

Symbol	Description
A <sub>0</sub> to A <sub>18</sub>	Address input
DQ <sub>1</sub> to DQ <sub>16</sub>	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V <sub>DD</sub>	+3.3 V power supply
V <sub>SS</sub>	Ground
NC	No connect

### Block Diagram



**512K x 16 Async SRAM in 119-bump, 14 mm x 22 mm—Top View (Package B)**

	1	2	3	4	5	6	7
A	NC	A15	A14	A16	A13	A12	NC
B	NC, V <sub>SS</sub>	A11	A10	$\overline{CE}$	A9	A8	NC
C	NC	NC	V <sub>DD</sub> , NC	A17	V <sub>SS</sub> , NC	NC	NC
D	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC
E	DQ1	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	DQ16
F	DQ2	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	DQ15
G	DQ3	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	DQ14
H	DQ4	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	DQ13
J	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>
K	DQ5	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	DQ12
L	DQ6	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	DQ11
M	DQ7	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	DQ10
N	DQ8	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	DQ9
P	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC
R	NC	NC	NC	A18	NC	NC	NC
T	NC	A7	A6	$\overline{WE}$	A5	A4	NC, V <sub>SS</sub>
U	NC	A3	A2	$\overline{OE}$	A1	A0	NC

**Note:**

Bumps 1B, 7T, 3C, and 5C are actually NC's but should be wired 3C = V<sub>DD</sub> and 1B, 7T and 5C = V<sub>SS</sub> to assure compatibility with future versions.

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ <sub>1</sub> to DQ <sub>8</sub>	V <sub>DD</sub> Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	—
L	X	L	Write	I <sub>DD</sub>
L	H	H	High Z	—

X: "H" or "L"

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>DD</sub>	-0.5 to +4.6	V
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5 (≤ 4.6 V max.)	V
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	1.5	W
Storage temperature	T <sub>STG</sub>	-55 to 150	°C

**Note:**

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/10/12	V <sub>DD</sub>	3.0	3.3	3.6	V
Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T <sub>Ac</sub>	0	—	70	°C
Ambient Temperature, Industrial Range	T <sub>Ai</sub>	-40	—	85	°C

**Notes:**

- Input overshoot voltage should be less than V<sub>DD</sub> +2 V and not exceed 20 ns.
- Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

**Capacitance**

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	10	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	7	pF

**Notes:**

1. Tested at  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$
2. These parameters are sampled and are not 100% tested

**DC I/O Pin Characteristics**

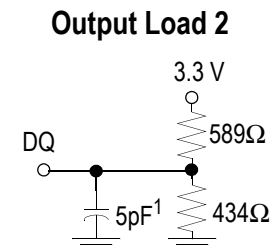
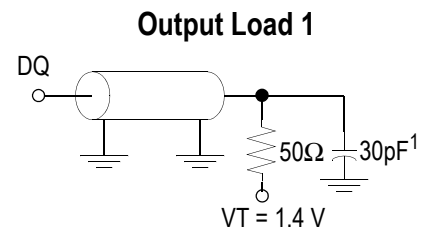
Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	$I_{IL}$	$V_{IN} = 0\text{ to }V_{DD}$	-2 $\mu\text{A}$	2 $\mu\text{A}$
Output Leakage Current	$I_{OL}$	Output High Z, $V_{OUT} = 0\text{ to }V_{DD}$	-1 $\mu\text{A}$	1 $\mu\text{A}$
Output High Voltage	$V_{OH}$	$I_{OH} = -4\text{ mA}$	2.4	
Output Low Voltage	$V_{OL}$	$I_{OL} = +4\text{ mA}$		0.4 V

**Power Supply Currents**

Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	$I_{DD}$	$\bar{E} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0\text{ mA}$	160 mA	130 mA	115 mA	180 mA	150 mA	135 mA
Standby Current	$I_{SB1}$	$\bar{E} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	60 mA	50 mA	50 mA	80 mA	70 mA	70 mA
Standby Current	$I_{SB2}$	$E \geq V_{DD} - 0.2\text{V}$ All other inputs $\geq V_{DD} - 0.2\text{V}$ or $\leq 0.2\text{V}$	20 mA			40 mA		

**AC Test Conditions**

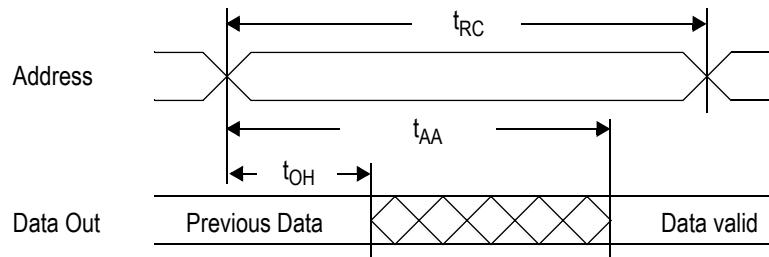
Parameter	Conditions
Input high level	$V_{IH} = 2.4\text{ V}$
Input low level	$V_{IL} = 0.4\text{ V}$
Input rise time	$t_r = 1\text{ V/ns}$
Input fall time	$t_f = 1\text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	<b>Fig. 1 &amp; 2</b>


**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$ .

**AC Characteristics**
**Read Cycle**

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	8	—	10	—	12	—	ns
Address access time	$t_{AA}$	—	8	—	10	—	12	ns
Chip enable access time ( $\overline{CE}$ )	$t_{AC}$	—	8	—	10	—	12	ns
Output enable to output valid ( $\overline{OE}$ )	$t_{OE}$	—	3.5	—	4	—	5	ns
Output hold from address change	$t_{OH}$	3	—	3	—	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	$t_{LZ}^*$	3	—	3	—	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}^*$	0	—	0	—	0	—	ns
Chip disable to output in High Z ( $\overline{CE}$ )	$t_{HZ}^*$	—	4	—	5	—	6	ns
Output disable to output in High Z ( $\overline{OE}$ )	$t_{OHZ}^*$	—	3.5	—	4	—	5	ns

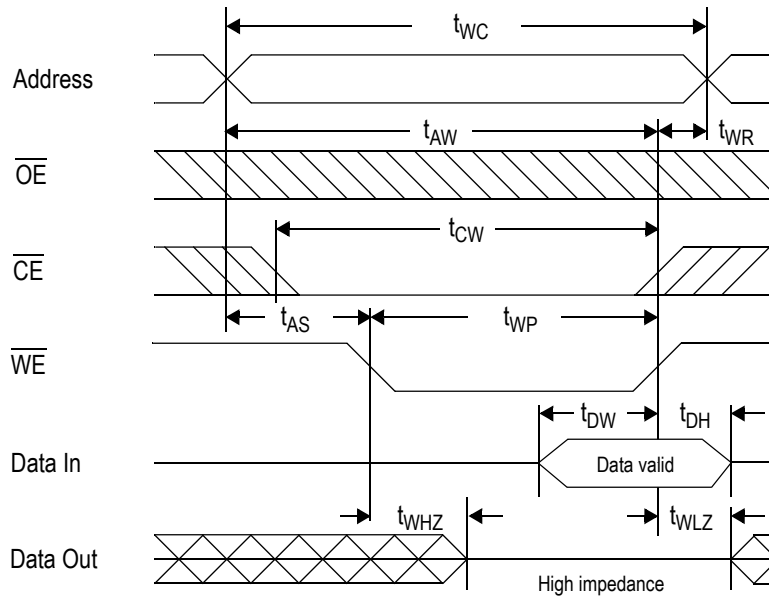
**Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$** 


\* These parameters are sampled and are not 100% tested

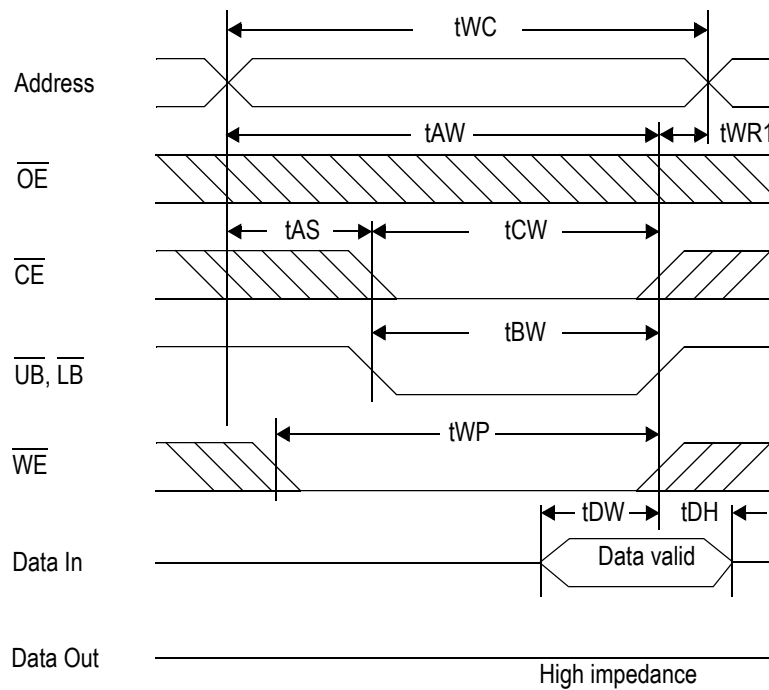
**Write Cycle**

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	8	—	10	—	12	—	ns
Address valid to end of write	$t_{AW}$	5.5	—	7	—	8	—	ns
Chip enable to end of write	$t_{CW}$	5.5	—	7	—	8	—	ns
Data set up time	$t_{DW}$	4	—	5	—	6	—	ns
Data hold time	$t_{DH}$	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}$	5.5	—	7	—	8	—	ns
Address set up time	$t_{AS}$	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	$t_{WR}$	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	$t_{WR1}$	0	—	0	—	0	—	ns
Output Low Z from end of write	$t_{WLZ}^*$	3	—	3	—	3	—	ns
Write to output in High Z	$t_{WHZ}^*$	—	3.5	—	4	—	5	ns

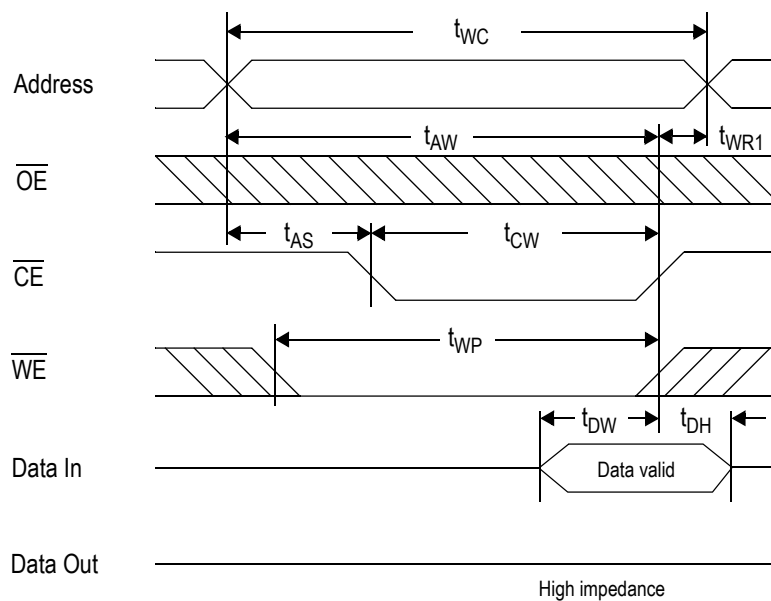
**Write Cycle 1:  $\overline{WE}$  Controlled**



**Write Cycle 3:  $\overline{UB}$ ,  $\overline{LB}$  control**



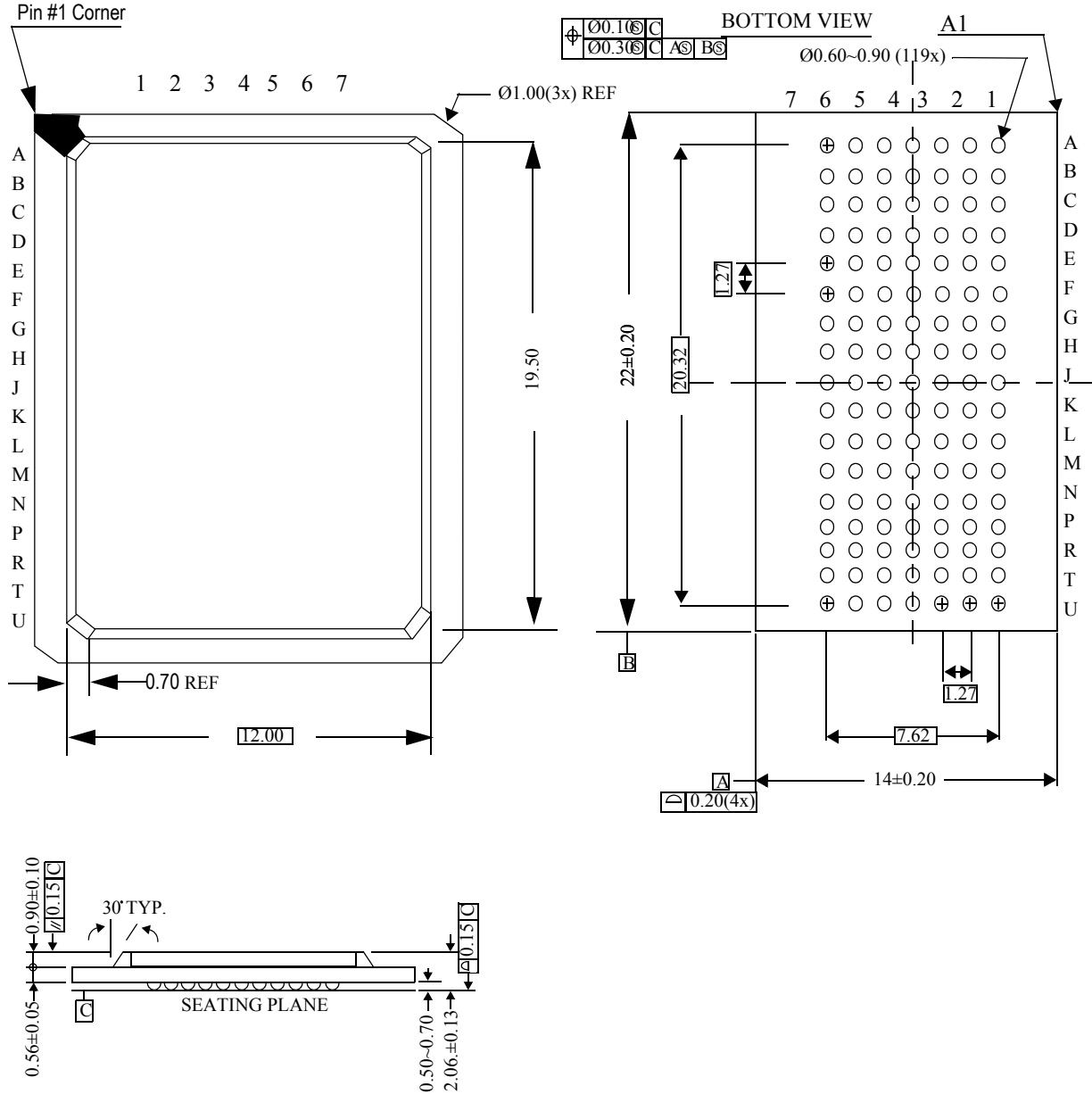
Write Cycle 2:  $\overline{\text{CE}}$  Controlled





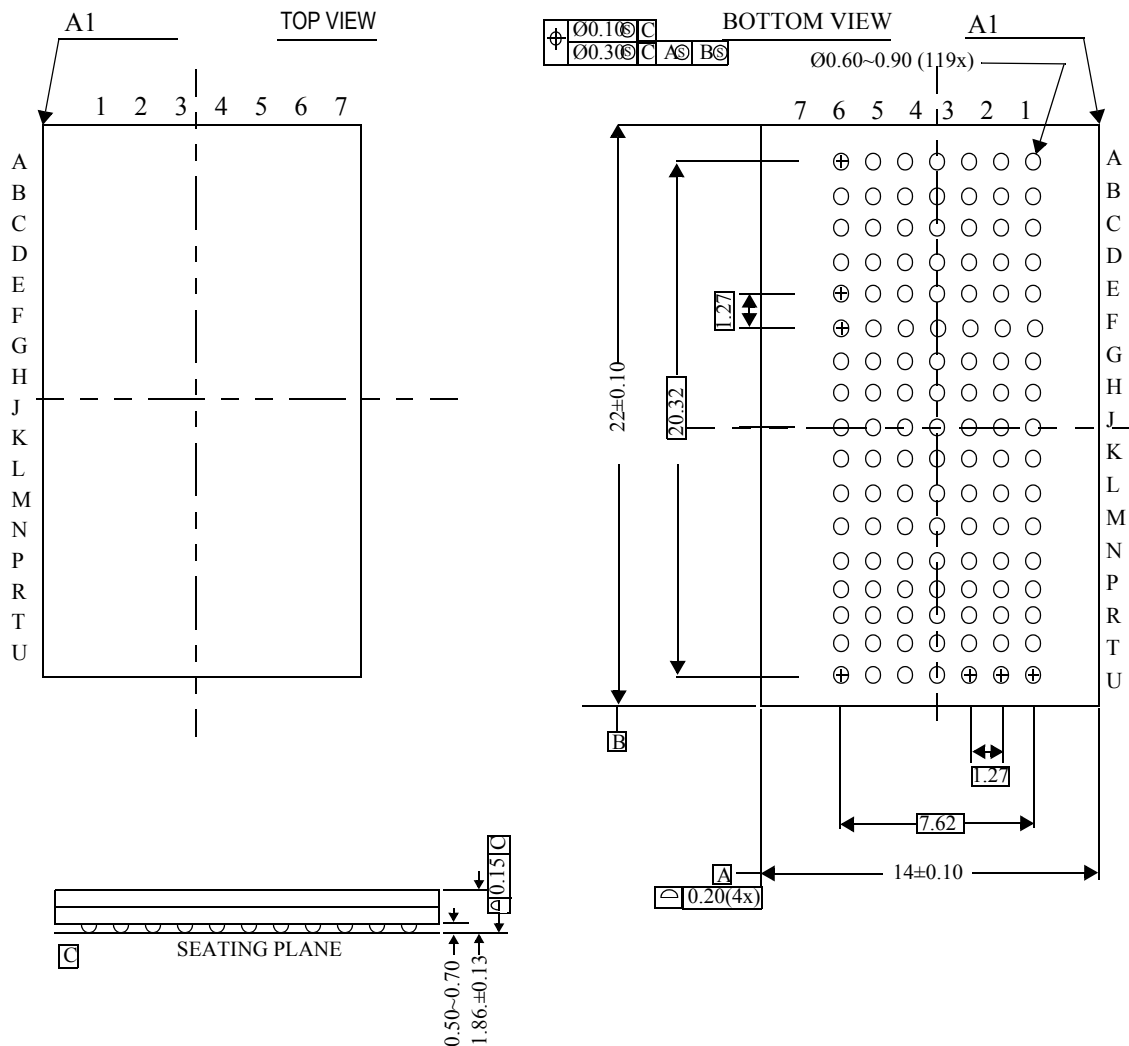
Package Dimensions—119-Bump FPBGA (Package B, Variation 1)

(Date Code: yyww.31)



Package Dimensions—119-Bump FPBGA (Package B, Variation 2)

(Date Code: yyww.3H)



**Ordering Information**

<b>Part Number<sup>1</sup></b>	<b>Package</b>	<b>Access Time</b>	<b>Temp. Range</b>	<b>Status</b>
GS78116AB-8	119-Bump BGA <sup>2</sup>	8 ns	Commercial	
GS78116AB-10	119-Bump BGA <sup>2</sup>	10 ns	Commercial	
GS78116AB-12	119-Bump BGA <sup>2</sup>	12 ns	Commercial	
GS78116AB-8I	119-Bump BGA <sup>2</sup>	8 ns	Industrial	
GS78116AB-10I	119-Bump BGA <sup>2</sup>	10 ns	Industrial	
GS78116AB-12I	119-Bump BGA <sup>2</sup>	12 ns	Industrial	
GS78116AGB-8	RoHS-compliant 119-Bump BGA <sup>2</sup>	8 ns	Commercial	
GS78116AGB-10	RoHS-compliant 119-Bump BGA <sup>2</sup>	10 ns	Commercial	
GS78116AGB-12	RoHS-compliant 119-Bump BGA <sup>2</sup>	12 ns	Commercial	
GS78116AGB-8I	RoHS-compliant 119-Bump BGA <sup>2</sup>	8 ns	Industrial	
GS78116AGB-10I	RoHS-compliant 119-Bump BGA <sup>2</sup>	10 ns	Industrial	
GS78116AGB-12I	RoHS-compliant 119-Bump BGA <sup>2</sup>	12 ns	Industrial	

**Notes:**

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number.  
For example: GS78116AB-12T
- Please see pages 8 and 9 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.

**Revision History**

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS78116AB_r1		• Creation of new datasheet
GS78116AB_r1_01	Content	• Added AC specifications to datasheet
GS78116AB_r1_01; GS78116AB_r1_02	Content/Format	• Updated format • Added variation information to package mechanical
GS78116AB_r1_02; GS78116AB_r1_03	Content	• Added Variation 2 119 BGA to datasheet • Added date codes to mechanicals
GS78116AB_r1_03; GS78116AB_r1_04	Content	• Added RoHS-compliant package information • (Rev1.04a: Added missing Write Cycle 3 timing diagram)