SigmaQuad™ and SigmaDDR™ Power-Up

Introduction

The SigmaQuad™ and SigmaDDR™ family of SRAMs, including Type-II, Type-II+, and Type IIIe, include a DLL (Delay Locked Loop) for output timing control. The DLL synchronizes the data valid window to the input clocks. This application note presents two approaches to power-up timing for these devices.

Start up of device's power supplies

All SigmaQuad and SigmaDDR devices require two power sources and one low current reference voltage. The power supplies are V_{DD} and V_{DDQ} and the reference voltage input is V_{REF}. The ideal power-up sequence for these three inputs is:

1. V_{DD}—the highest voltage
2. V_{DDQ}—the middle voltage
3. V_{REF}—the lowest voltage

Some board layouts source V_{DD} and V_{DDQ} from the same power supply and may supply V_{REF} via V_{DDQ} through a resistor network. This board design approach is generally acceptable, since neither V_{DDQ} nor V_{REF} are expected to exceeded V_{DD}.

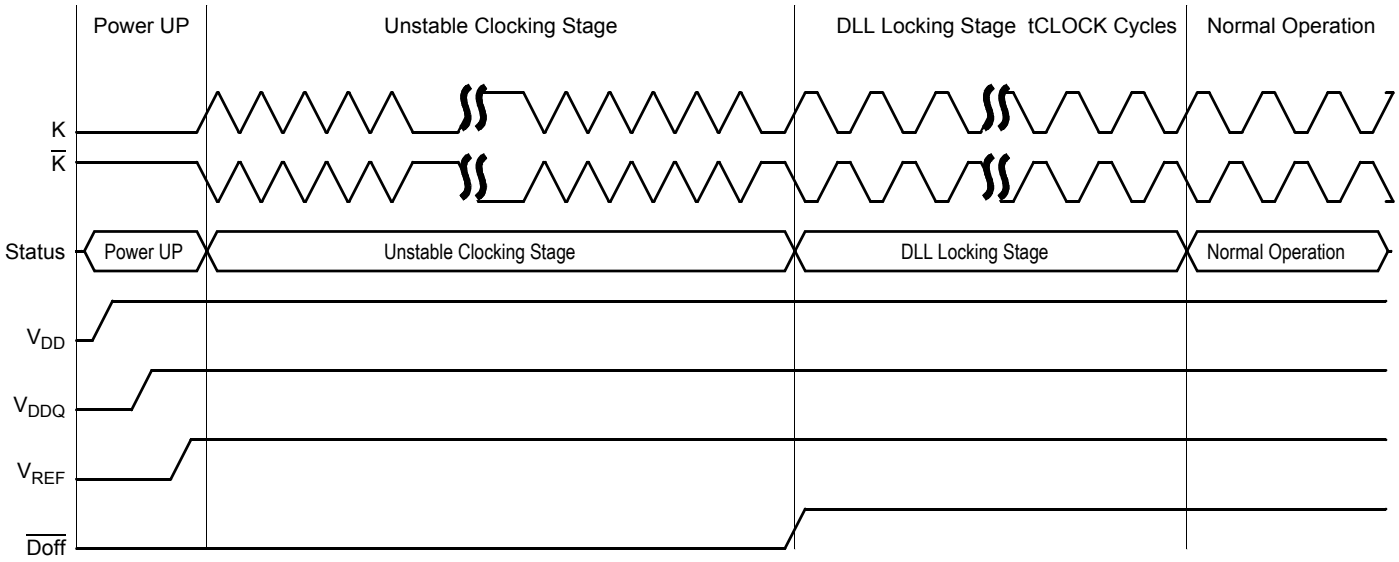
Clock starting and $\overline{\text{Doff}}$ pin

SigmaQuad and SigmaDDR SRAMs utilize automatic power-up logic reset circuits designed to allow the RAMs to tolerate adverse logic input conditions that may exist during and just after device power-up. Although the automatic power-up reset logic will allow the RAM to power-up and sync to the applied clock, a few extra steps can be taken at power-up to minimize power consumption and noise on the board during start-up.

In many cases, after power-up the SRAM's input clocks are either pulled High or Low, near or equal to V_{REF}, or free running. In fact, the same can be said of any of the RAM's input pins. During and after power-up, the host device driving the SRAMs may drive the clock input pins and the $\overline{\text{Doff}}$ pin Low or High or may oscillate between logic High and logic Low at some unpredictable rate because the input is either floating metastable or held to V_{REF} by a termination resistor. The RAM's power-up reset circuits are designed to prevent these conditions from causing logic problems, but these unpredictable signals can cause power consumption on the RAM and unnecessarily generate noise on the board during the power-up interval. One way to avoid these problems is for the host chip to hold the RAM inputs to a fixed logic level during power-up, but that is often not possible. Controlling the $\overline{\text{Doff}}$ pin can mitigate many of the effects of metastable inputs at power-up.

Best design practice is to have the host device controlling the SRAM drive the $\overline{\text{Doff}}$ pin Low (or to install a weak pull-down on the $\overline{\text{Doff}}$ pin to keep it Low if the host device cannot drive it Low), in order to turn the DLL off during power up and when the clocks are unstable. Once the host device is fully initialized and producing stable SRAM clocks, it can then drive the $\overline{\text{Doff}}$ pin High in order to turn the DLL on. This allows the SRAM's DLL to lock onto the stable input clock as quickly and efficiently as possible.

SigmaQuad/SigmaDDR Power-Up, DLL Controlled



However, since control of $\overline{\text{Doff}}$ can prove difficult or impossible during power-up, the SigmaQuad and SigmaDDR family is designed to automatically recover from excessively unstable or out-of-range clocks even if the $\overline{\text{Doff}}$ pin is active High during any or all of the power-up sequence. In these cases, once input clocks are stabilized within the RAM's required frequency and duty cycle range the RAM automatically initiates DLL synchronization and can begin normal operations after the required sync interval given in the datasheet.

SigmaQuad/SigmaDDR Power-Up, DLL On