GSI's Synchronous Burst/NBT SRAMs Bridge the Gap Between Computer and Netcom Applications

Introduction

The most common reason for SRAM memory in computers is to support cache applications. The most common reason for SRAM memory in Netcom is to support buffering and high speed lookup. Each of these applications has different challenges and requirements. Cache tends to be relatively small, and is typically accessed in chunks called bursts. Netcom applications tend to use large memories, which continuously write and read in random patterns. GSI's Synchronous Burst/NBT SRAMs bridge the gap between legacy SRAMs designed for computer applications and SigmaRAMs designed specifically to solve Netcom problems.

High Performance		
Clock Rate	Bus Width	Read/Write Bandwidth
200 MHz	x18	3.6Gb/s
	x36	7.2Gb/s
	x72	14.4Gb/s
250 MHz	x18	4.5Gb/s
	x36	9.0Gb/s
	x72	18.0Gb/s
300 MHz	x18	5.4Gb/s
	x36	10.8Gb/s
	x72	21.6Gb/s

Applications

Burst/NBT SRAMs from GSI come in a variety of densities from 1Mb to 36Mb. Built for speed, with pipelined performance up to 300 MHz, they also have low power consumption. Both computer and network designers will also appreciate the available bus widths from x18 to x72. The combination of high clock rate and wide bus width gives GSI Technology Synchronous/NBT SRAMs a throughput performance unsurpassed in the industry. The burst protocol (programmable in linear or interleaved mode) makes the burst RAMs a perfect choice for fast cache applications. The NBT protocol (allows penalty free back to back reads and writes) is a feature of extreme importance when processing high speed data streams.

Ultra Low Power Consumption (x36)		
Clock Rate	Current	Power
200 MHz	260 mA	468 mW
250 MHz	315 mA	567 mW
300 MHz	378 mA	680 mW

Features and Benefits

Aside from high performance and low power, Synchronous Burst/ NBT SRAMs also support many additional features, such as flow through and pipelined operation in a single part, IEEE 1149.1 JTAG compliance, programmable output impedance, and SCD or DCD modes. All Synchronous Burst/NBT SRAMs support the legacy burst protocol for efficient cache line fills. Industry standard packaging is available in TQFP or BGA.

Features	Benefits
300 MHz clock	High performance
x18/x36/x72	High throughput
Low power	Less power = Less heat
1.8 or 2.5 volt operation	Adaptable for legacy or advanced sockets
NBT protocol	No penalty reads/writes
Burst protocol	Supports cache line fills
Programmable Pipeline/Flow Through mode	One part, two applications
Programmable Linear/Intel Burst mode	Adaptable to any environment
Global and Byte writes	Configurable for special applications
3 chip enables	Easily expandable
JEDEC packaging	Purchase with confidence, 2nd sourcing guaranteed
JTAG	Adaptable for self-test protocols