Using ByteSafe™ SRAMs in Parity and Non-Parity Applications

Introduction

GSI's ByteSafe™ technology opens a new front in the battle for highly reliable data. Although parity bit storage has been around for as long as digital memory, learning whether data arrived correctly or if it was lost in storage has remained all but impossible. Today, in networking and communications applications, with so much memory being used outside it's traditional role supporting a general-purpose processor, the wait to discover a written error can become painfully long. ByteSafe™ parity RAMs address this need.

Application

GSI currently offers 8M and 16M synchronous SRAMs with or without ByteSafe™ technology. GSI differentiates their normal x16/x32 and x18/x36 from the ByteSafe™ SRAMs by the part number. When ordering a GSI SRAM with ByteSafe™ make sure the part number starts with GS881xx, GS882xx, GS8161xx, or GS8162xx.

The ByteSafe™ technology is simple. In x32/x16 mode ($\overline{PE}$ = 1), an SRAM with ByteSafe™ features a parity encoding and checking function. During the write cycle, parity is generated by the device and stored along with the written data. Since the RAM is in x32/16 mode, it is assumed that there is no facility in the system for parity checking. The ByteSafe™ circuitry checks read parity and if needed, generates an error on the Parity Error Out ($\overline{QE}$) pin on the second clock (CK) cycle. If the RAM is being operated in flow through mode ($\overline{FT}$ = 0), the error signal is clocked on the next cycle. In x32/x16 mode the device does not drive the ninth data output, even though the internal ByteSafe™ parity encoding has been activated.

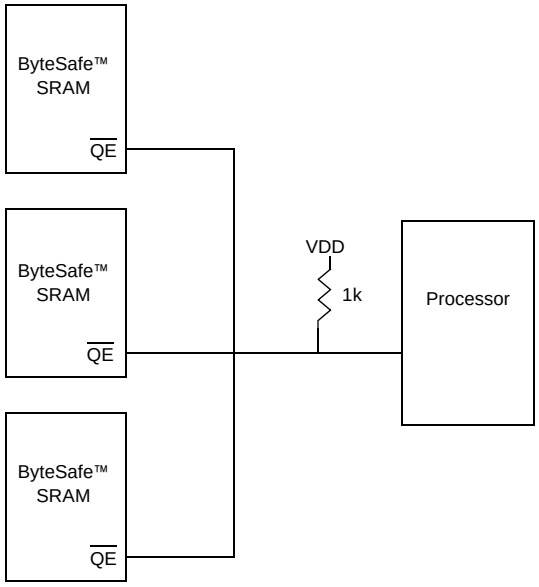
In x18/x36 mode ($\overline{PE}$ = 0), incoming byte parity encoded data is routed to a parity checking circuit at the same time that it is sent to the memory array. Any error detected is captured in the Parity Error Out ($\overline{QE}$) signal on the second rising edge of the RAM's clock (CK). If the RAM is being operated in flow through mode ($\overline{FT}$ = 0) the error signal is driven immediately.

ByteSafe™ RAMs have a Data Parity (DP) mode select pin because incoming parity data may be encoded even (DP = 1) or odd (DP = 0).

The Parity Error Out signal uses an open drain output driver, allowing multiple RAMs to share a common pull up resistor.

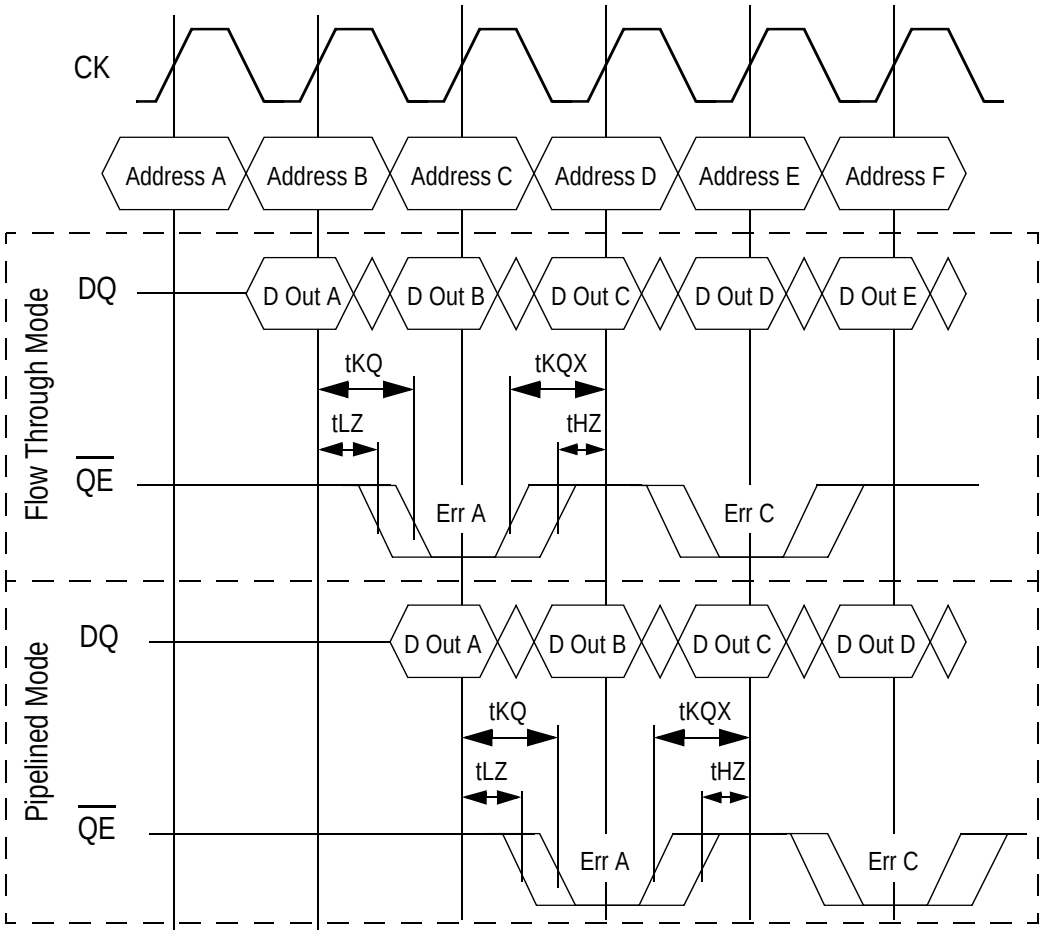
Summary

ByteSafe™ RAMs derive their power and utility in a system because they bring parity to systems that otherwise would go unchecked. They also offer designers of failure-hardened systems the first opportunity to immediately monitor the validity of written data eliminating the need for time-consuming parity checks and shortening lengthy system debugs.



Open Drain Output Driver with Pull-up

x16/x32 Mode ($\overline{PE}$ = 1) Read Parity Error Output Timing Diagram



x18/x36 Mode ($\overline{PE}$ = 0) Write Parity Error Output Timing Diagram