SigmaQuad/DDR IIIe/IVe SRAM Overview

Introduction

GSI's SigmaQuad and SigmaDDR IIIe and IVe families of synchronous SRAMs have been designed to deliver significantly greater performance than that provided by the older-generation II and II+ families (the highest performance commercially-available synchronous SRAMs prior to the advent of the IIIe family). Both the IIIe and IVe families come in 3 functional variations—Quad B2 (Separate I/O, Burst of 2), Quad B4 (Separate I/O, Burst of 4), and DDR B2 (Common I/O, Burst of 2), and in 2 configurations—x18 and x36.
The Quad B2 device can execute two operations, a Read and a Write, per cycle, whereas the Quad B4 and DDR B2 devices can only execute one operation, a Read or a Write, per cycle. Consequently, at a given operating frequency, the Quad B2 device provides twice the *transaction rate* of the Quad B4 and DDR B2 devices, with equivalent per-pin *data bandwidth*. And as transaction rate has become the primary driver of SRAM performance requirements in the Networking & Telecom markets, Quad B2 performance is the primary focus of the IIIe and IVe families.

Type IIIe Family Overview

The IIIe family was defined to double the maximum transaction rate available in the II and II+ families. It begins at 72Mb density (in production now), and to help achieve the performance targets it includes the following new features previously unavailable in the II and II+ families:

- A lower core voltage (V_{DD}) of 1.35 V, to reduce power consumption (compared to 1.8 V in II and II+ devices).
  Note: Core voltage is reduced further yet, to 1.2V, in the 144Mb and 288Mb IIIe devices.

- A lower I/O voltage (V_{DDQ}) of 1.2 V (HSTL), to improve signal integrity and reduce power consumption (compared to 1.5 V in II and II+ devices).
  Note: 1.5 V HSTL I/O voltage is also supported, for those applications that cannot utilize a 1.2 V HSTL I/O interface.

- Dedicated Input Clocks for Write Data capture, to make it easier to meet setup and hold time requirements across all synchronous inputs.

- Highly-configurable On-Die Termination (ODT), on all synchronous high speed inputs (i.e., Clocks, Data, Address, and Control).
  Note: Some Type II+ devices also offer ODT, but only on a subset of the synchronous inputs, and with little configurability.

- Configurable Read Latency (RL)—either 2 cycles or 3 cycles.
  Note: The 2 cycle RL option is discontinued in the 144Mb and 288Mb IIIe devices.

- A new 260p BGA package, for better signal integrity. The new package and pinout reduce pin inductance considerably, compared to the 165p BGA package used in the older-generation II and II+ devices. And lower pin inductance directly equates to better signal integrity.

This combination of new package and features enables all 3 functional variations in the 72Mb IIIe family to operate up to 675 MHz and provide a per-pin data bandwidth up to 1.35Gb/s (gigabits per second), and enables the Quad B2 device to provide a transaction rate up to 1.35GT/s (giga-transactions per second).

In comparison, at the time the 72Mb IIIe family was introduced (in 2010), the fastest Quad B2 devices were 333 MHz in the II family (equating to 0.66 Gb/s per-pin data bandwidth and 0.66 GT/s transaction rate), and the fastest Quad B4 and DDR B2 devices were 550 MHz in the II+ family (equating to 1.1Gb/s per-pin data bandwidth and 0.55GT/s transaction rate). So the 72Mb IIIe family increased per-pin data bandwidth by 22% (from 1.1Gb/s to 1.35Gb/s in Quad B4 and DDR B2 devices), and more than doubled transaction rate (from 0.66GT/s to 1.35GT/s in Quad B2 devices), compared to the II and II+ family.

450 MHz Quad B2 devices (in the II+ family) and 633 MHz Quad B4 and DDR B2 devices (in the II+ family) have since been announced, but they still fall short of the performance levels achieved by the IIIe family, especially the transaction rate in the Quad B2 device.

The 144Mb and 288Mb versions of the IIIe family are in design now.

Type IVe Family Overview

The IVe family was defined to double the maximum transaction rate available in the IIIe family. It begins at 144Mb density (in design now), and to help achieve the performance targets it includes the following new architecture and features previously unavailable in the IIIe family:

- The memory array is segmented into multiple logical banks, in order to double the performance over that achieved by the IIIe family.
  Note: The memory array in IIIe devices is architected as a single logical bank, and the internal array access that occurs in response to the current Read or Write operation always completes before the internal array access that occurs in response to the next Read or Write operation begins. Consequently, there are no address restrictions when initiating a sequence of Read and Write operations to IIIe devices. However, 675 MHz is about the maximum that can be achieved with single bank architecture in a Quad B2 device. Therefore, to double performance, the memory array in IVe devices is segmented into multiple logical banks, and the internal array access that occurs in response to the current Read or Write operation does not necessarily complete before the internal array access that occurs in response to the next Read or Write operation begins. Consequently, there are addressing restrictions when initiating a sequence of Read and Write operations in IVe devices, such that different logical banks are accessed when the array accesses that occur in response to consecutive Read and Write operations overlap. The exact restrictions are defined in the product datasheets; they are more complex in Quad B2 devices than in Quad B4 and DDR B2 devices because Quad B2 devices can execute two operations per cycle whereas Quad B4 and DDR B2 devices can only execute one operation per cycle.
- Programmable Mode Registers, to expand and simplify device configuration.
- Special Loopback Modes, for per-pin timing training of Address inputs, Control inputs, and Data outputs.
  Note: After Address inputs, Control inputs, and Data outputs are trained, Data inputs are easily trained via normal Write and Read operations. It is expected that such signal training will be mandatory at the maximum signal rates available in IVe devices (~2.8Gb/s).
- An on-chip PLL, to help maximize Data output valid windows.
- Support for 1.2V POD I/O with optional Data Inversion, in addition to 1.2V HSTL I/O, for better signal integrity and greater application flexibility. POD I/O signaling with Data Inversion reduces by half the number of Data pins that can transition in the same direction in any given cycle, thereby reducing SSO noise and improving signal integrity compared to HSTL I/O signaling.
  Note: Support for 1.5V HSTL I/O is discontinued in the IVe family.
- Configurable Read Latency (RL) – either 5 cycles or 6 cycles.

This combination of new architecture and features enables all 3 functional variations in the 144Mb IVe family to operate up to ~1400 MHz and provide a per-pin data bandwidth up to ~2.8Gb/s, and enables the Quad B2 device to provide a transaction rate up to ~2.8GT/s.

Feature Comparison Table

	IIIe												IVe						Units
Density	72 Mb						144 Mb			288 Mb			144 Mb						
Process Technology	65 nm						40 nm			40 nm			40 nm						
Bank Architecture	Single-Bank						Single-Bank			Single-Bank			Multi-Bank						
Organization	x18 / x36						x18 / x36			x18 / x36			x18 / x36						
Device Types	Quad		DDR	Quad		DDR	Quad		DDR	Quad		DDR	Quad		DDR	Quad		DDR	
	B2	B4	B2	B2	B4	B2	B2	B4	B2	B2	B4	B2	B2	B4	B2	B2	B4	B2	
Write Latency	0	1	1	0	1	1	0	-1	1	0	1	1	0	-1	0	0	-1	0	cycles
Read Latency	2			3			3			3			5			6			cycles
Operating Frequency (max)	450			675			~700			~500	~633		~1050			~1400			MHz
On-Chip ECC	Yes						Yes			No			Yes						
On-Chip DLL / PLL	DLL						PLL			DLL			PLL						
Read Data aligned to Input Clocks	Yes						Yes			Yes			Yes						
Read Data aligned to Echo Clocks	Yes						Yes			Yes			Yes						
Separate Input Clocks for Write Data Capture	Yes						Yes			Yes			Yes						
Low-Power NOP Mode	Yes						No			No			No						
Configuration Registers	No						No			No			Yes						
Loopback Address & Control Timing Training	No						No			No			Yes						
Core Voltage (V_{DD})	1.3 V/1.35 V						1.2 V/1.25 V			1.2 V/1.25 V			1.2 V/1.25 V						
1.5 V HSTL I/O	Yes						Yes			Yes			No						
1.2 V HSTL I/O	Yes						Yes			Yes			Yes						
1.2 V POD I/O, with optional Data Inversion	No						No			No			Yes						

The graphic opposite depicts the pinout for x36 Quad B2/B4 IIIe/ IVe devices. In x36 DDR B2 IIIe/IVe devices, all pins labeled "D In" are unused, and all pins labeled "Q Out" are "DQ In/Out".

The graphic opposite depicts the pinout for HSTL I/O IIIe/IVe devices. In POD I/O IVe devices:

1. A4, A10, Y4, Y10: are "DINV In" pins in Quad B2/B4 devices, and unused in DDR B2 devices.
2. A2, A12, Y2, Y12: are "QINV In" pins in Quad B2/B4 devices, and "DQINV In/ Out" pins in DDR B2 devices.

The double-line boundary around 13 pin locations in the graphic opposite highlight pin locations whose definitions vary slightly between the 72Mb IIIe, 144Mb IIIe, 288Mb IIIe, and 144Mb IVe devices.

The table on the following page provides a detailed explanation of those differences. This information is intended to help users design a single SRAM controller interface and system board that can accommodate a combination of these IIIe and IVe devices.

Pin	IIIe			IVe	Comments
	72Mb	144Mb	288Mb	144Mb	
9D	NC (144Mb)	SA	SA	SA	In 72Mb device, it is unused and reserved for 144Mb address pin. In 144Mb & 288Mb devices, it is used as an address pin.
7D	NC (288Mb)	NC (288Mb)	SA	NC (288Mb)	In 72Mb & 144Mb devices, it is unused and reserved for 288Mb address pin. In 288Mb devices, it is used as an address pin.
5U	NU	NC (576Mb)	NC (576Mb)	NC (576Mb)	In 72Mb devices, it is connected to the die but unused; it can be left unconnected or tied Low. In 144Mb & 288Mb devices, it is unused and reserved for 576Mb address pin.
9U	NU	NC (1152Mb)	NC (1152Mb)	NC (1152Mb)	In 72Mb devices, it is connected to the die but unused; it can be left unconnected or tied Low. In 144Mb & 288Mb devices, it is unused and reserved for 1152Mb address pin.
9N	MCH	MCH	MCH	MCL	In IIIe devices, it must be tied High. In IVe devices, it must be tied Low.
5A	MCL	NC (RSVD)	NC (RSVD)	NC (RSVD)	In 72Mb devices, it must be tied Low. In 144Mb & 288Mb devices, it is unused and reserved for future use; it can be left unconnected or tied Low or High.
5B	MVQ	MVQ	MVQ	MCL	In IIIe devices, it is used to configure the device for either 1.2 V I/O (MVQ = 0) or 1.5 V I/O (MVQ = 1). In IVe devices, it must be tied Low.
7A	MCL	MCL	MCL	MRW	In IIIe devices, it must be tied Low. In IVe devices, it is used to enable Mode Register programmming (when High).
7U	ADZT1#	NC (RSVD)	NC (RSVD)	NC (RSVD)	In 72Mb devices, it is used to enable Low-Power NOP Mode (when High). In 144Mb & 288Mb devices, it is unused and reserved for future use; it can be left unconnected or tied Low or High.
5N	DLL	PLL	DLL	PLL	72Mb & 288Mb devices utilize an internal DLL, and this pin is used to enable/ disable it. 144Mb devices utilize an internal PLL, and this pin is used to enable/disable it.
7W	NC (RSVD)	RCS	NC (RSVD)	RCS	In 72Mb & 288Mb devices, it is unused and reserved for future use. In 144Mb devices, it should be connected to V_{SS} through a 2Kohm resistor. See Note 1 for more information.
6W	RLM0	MCL	MCL	MCL	In 72Mb devices, RLM[1:0] select between RL=2 (RLM[1:0] = 01) and RL=3 (RLM[1:0] = 10). In 144Mb & 288Mb devices, pin 6W must be tied Low. In 144Mb & 288Mb devices, pin 7Y is unused and reserved for future use; it can be left unconnected or tied Low or High. See Note 2 for more information.
7Y	RLM1	NC (RSVD)	NC (RSVD)	NC (RSVD)	

Notes:

1. In 144Mb devices, the RCS pin is used to provide an accurate current source to the PLL.
   In 144Mb IVe devices, it must be connected to VSS through a 2Kohm resistor.
   In 144Mb IIIe devices, it may be left unconnected, in which case a less accurate current source for the PLL is derived internally.
   The less accurate current source results in a narrower operating range for a given speed grade device, vs. when the RCS resistor is connected.
2. 144Mb & 288Mb IIIe devices only support RL=3; they do not utilize RLM Mode pins.
   144Mb IVe devices support multiple RLs via Mode Register bits; they do not utilize RLM Mode pins.

