Interfacing GSI Sync SRAMs to a Freescale MPC5554 microcontroller

Introduction

This application note will discuss interfacing a Freescale MPC5554 microcontroller with GSI Syncronous Burst SRAMs.

Compatibility

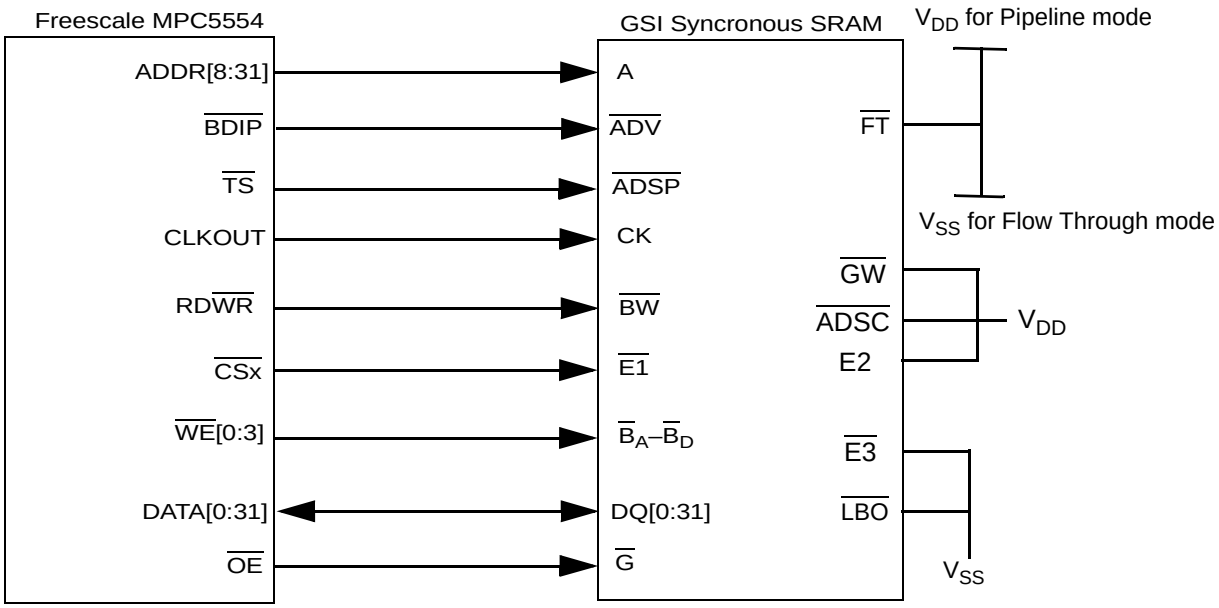
The Freescale MPC5554 is capable of interfacing with SRAMs that operate in either Flow Through or Pipeline mode, which is selectable by the addition of wait states in the MPC5554 read timing. The SRAMs must operate in a Late Write mode, where the data and byte writes are supplied one cycle after the write command is loaded. All of GSI's Synchronous Burst SRAMs are compatible with the Freescale MPC5554.

Interface

Figure 1 shows the basic connection between an MPC5554 and a GSI SRAM. The $\overline{FT}$ pin controls whether the SRAM operates in Pipeline mode or Flow Through mode. This pin needs to be tied to V_{SS} if the MPC is operating in a zero wait state Read Mode which is also referred to as Flow Through mode in the SRAM datasheet. The $\overline{FT}$ pin will need to be tied to V_{DD} if the MPC is operating in a one wait state Read Mode, which is also refered to as Pipline mode in the SRAM datasheet.

The MPC5554 microcontroller uses a Late Write protocol when perfroming L2 cache writes. This requires the design to use the $\overline{ADSP}$ pin to configure the SRAM to utilize a Late Write protocol.

Figure 1: Connection diagram



Timing Analysis

For all of the following timing diagrams, the GSI pin names are displayed on the left next to the MPC pin names. **Figure 2** is a timing diagram for L2 cache write. As seen in **Figure 2**, the addresses and $\overline{ADSP}$ signals are supplied on the first rising edge of clock for the beginnning of the write cycle and the write enable, byte writes, and data signals are supplied on the following rising edge of clock.

Figure 2: L2 cache write

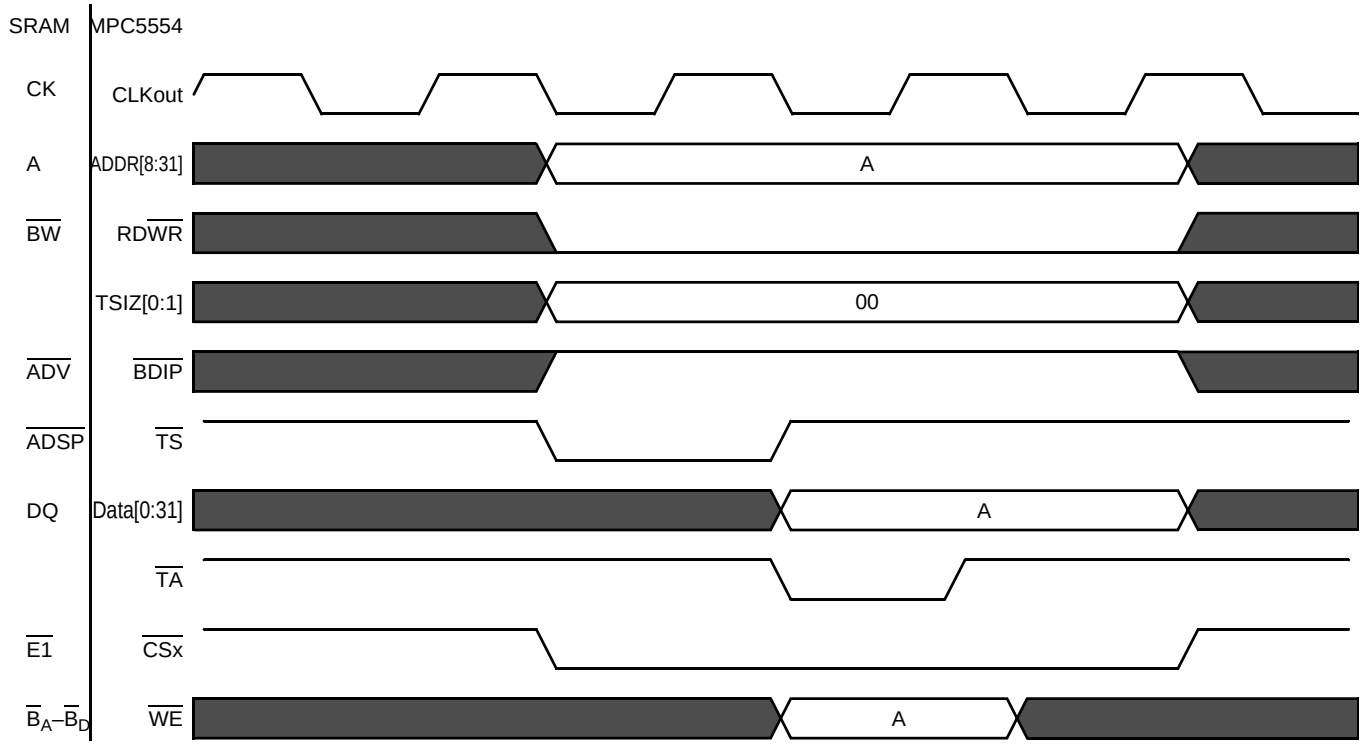


Figure 3 illustrates a flow through read which is also referenced as a zero wait state read. When the SRAM operates in Flow Through mode, the read command is clocked in and data is referenced to the same rising edge of clock.

Figure 3: Flow Through Mode or Zero Wait State Read

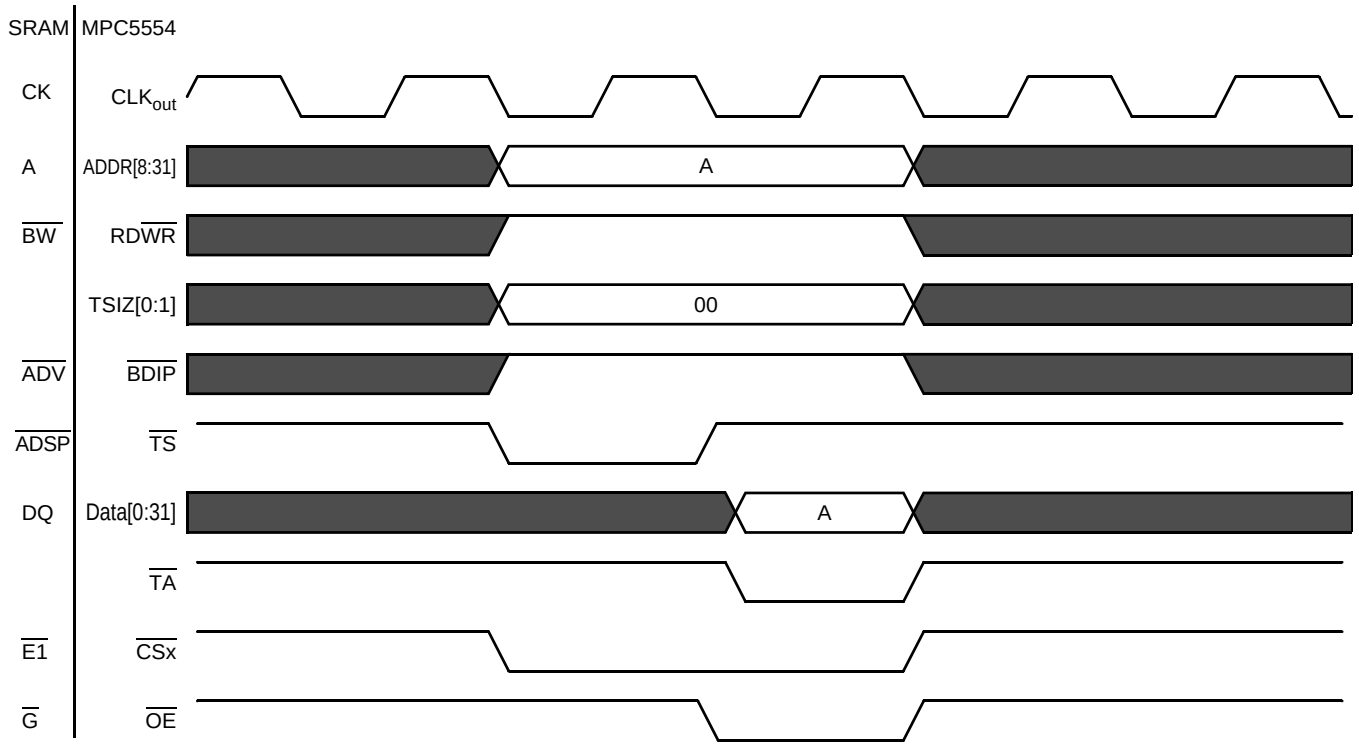


Figure 4 illustrates a flow through read cycle followed by a write cycle. One thing to notice is the required deslect cycle that is added between the read cycle and the write cycle. The deselect cycle is nessecary to allow the SRAM to get off the bus and the MPC to begin driving. If this cycle is omitted, there will be bus contention and it is possible that the MPC will not latch in correct data.

Figure 4: Flow Through Read Deselect Write

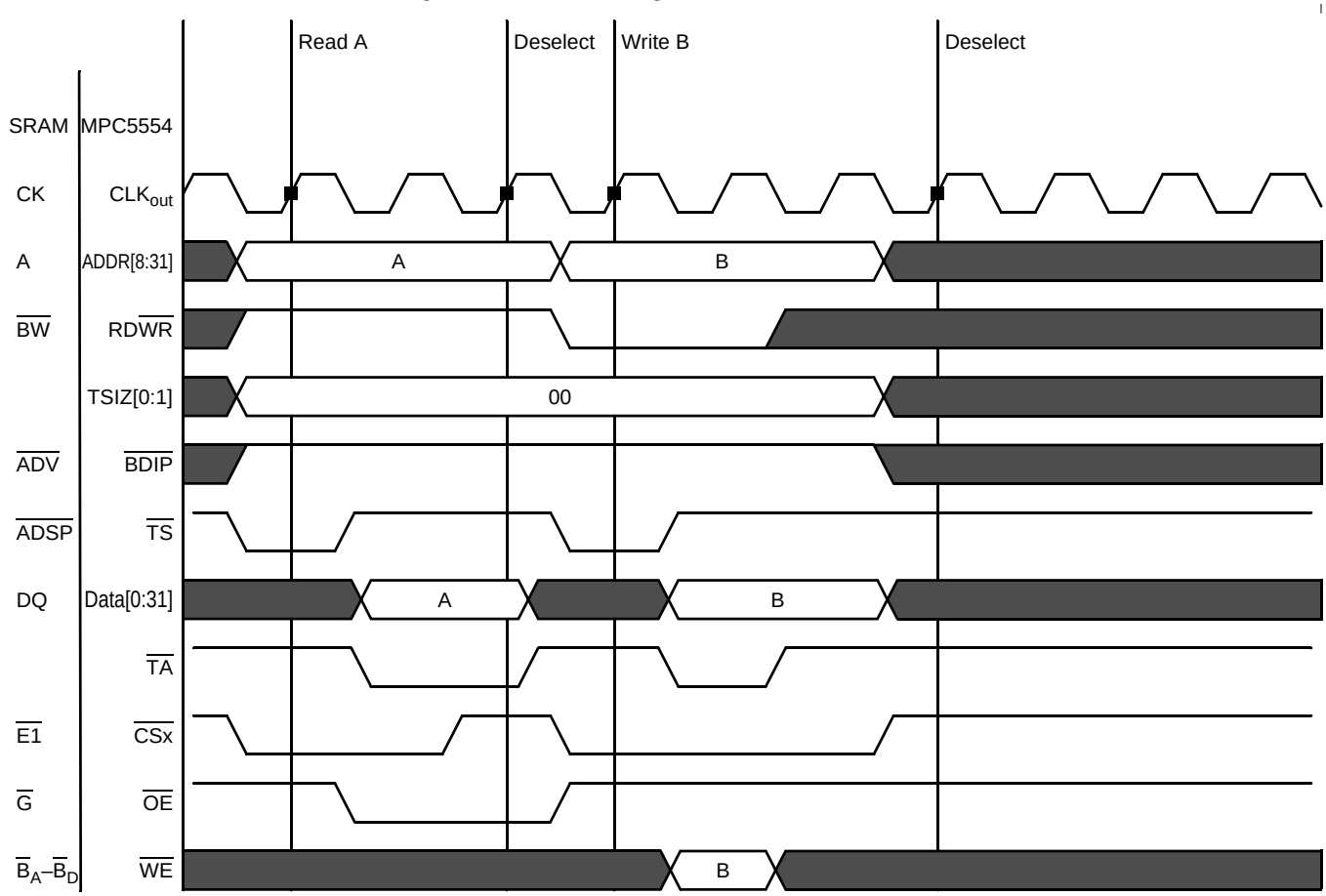
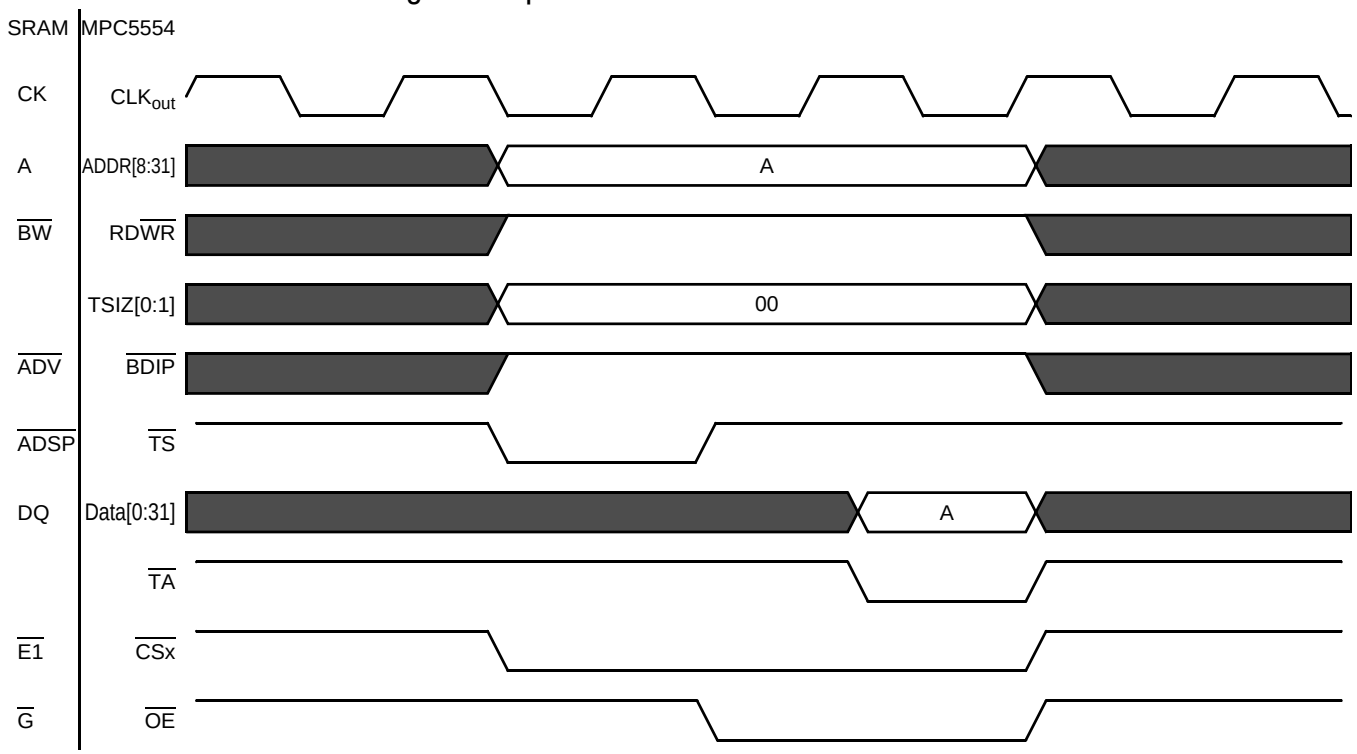


Figure 5 illustrates a pipeline read which is also referneced as a one wait state read. The read address is supplied on the rising edge of clock. On the next rising edge of the clock, data is driven out from the SRAM. The data is referenced to the second rising edge of clock.

Figure 5: Pipeline Read or One Wait State Read



Summary

The Freescale MPC5554 Microcontroller will interface with GSI Synchronous Burst SRAMs that are configured to operate in either Pipeline or Flow Through mode. The timing diagrams in this document bridged the gap between those provided in the Freescale documentation referencing the microcontroller signal names and GSI Synchronous Burst SRAM signal names. A designer using this document as a guide should be able to properly configure the interface to work with GSI Synchronous BurstRAM devices. If further questions still exist, please feel free to contact GSI Application Engineers at apps@gsitechnology.com.

