Interfacing GSI Sync SRAMs to a Freescale Multiplexed MPC567xF or PXR40xx Microcontroller

Introduction

This application note will discuss interfacing a Freescale MPC567xF microcontroller or the Freescale e200 PowerA PXR40xx microcontroller operating in Multiplexed mode with GSI Synchronous Burst SRAMs.

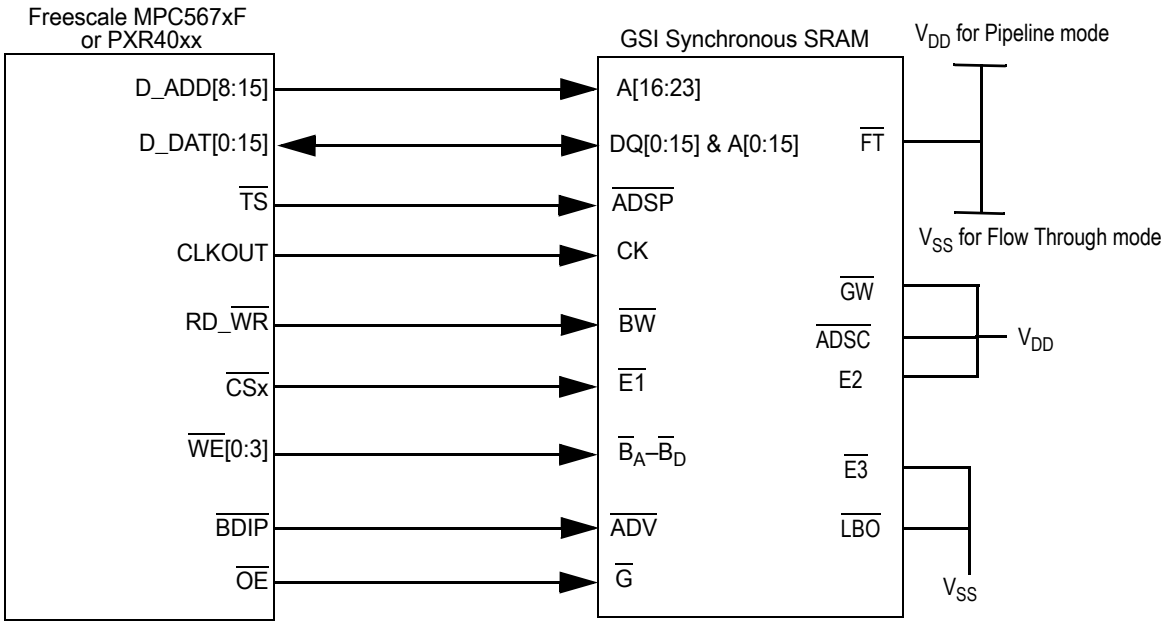
Compatibility

The Freescale MPC567xF and PXR40xx are capable of interfacing with SRAMs that operate in either Flow Through or Pipeline mode, which is selectable by the addition of wait states in the MPC567xF read timing. The SRAMs must operate in a Late Write mode, where the data and byte writes are supplied one cycle after the write command is loaded. All of GSI's Synchronous Burst SRAMs are compatible with the Freescale MPC567xF and PXR40xx.

Interfacing Using 16-bit Multiplexed Mode

Figure 1 shows the basic connection between either an MPC567xF or PXR40xx and a GSI SRAM. Both microcontrollers have been configured internally to interface with the SRAM using 16-bit Multiplexed mode. During an address cycle while operating in 16-bit Multiplexed mode, the microcontroller utilizes the Data Bus D_DAT[0:15] and parts of the address D_ADD[8:15] to issues addresses A[0:23]. The $\overline{FT}$ pin controls whether the SRAM operates in Pipeline mode or Flow Through mode. This pin needs to be tied to V_{SS} if the microcontroller is operating in a zero wait state Read mode, which is also referred to as Flow Through mode in the SRAM datasheet. The $\overline{FT}$ pin will need to be tied to V_{DD} if the microcontroller is operating in a one wait state Read mode, which is also referred to as Pipeline mode in the SRAM datasheet.

Figure 1: Connection diagram 16-bit Multiplexed mode



The MPC567xF and PXR40xx microcontrollers use a Late Write protocol when performing L2 cache writes. This requires the design to use the $\overline{ADSP}$ pin to configure the SRAM to utilize a Late Write protocol.

Timing Analysis

For all of the following timing diagrams, the GSI pin names are displayed on the left next to the microcontroller pin names. **Figure 2** is a timing diagram for L2 cache write. As seen in **Figure 2**, the addresses, supplied on D_ADD and D_DAT buses, and $\overline{\text{ADSP}}$ signals are supplied on the first rising edge of clock for the beginning of the write cycle and the write enable, byte writes, and data signals are supplied on the following rising edge of clock.

Figure 2: L2 Cache Write in 16-bit Multiplexed mode

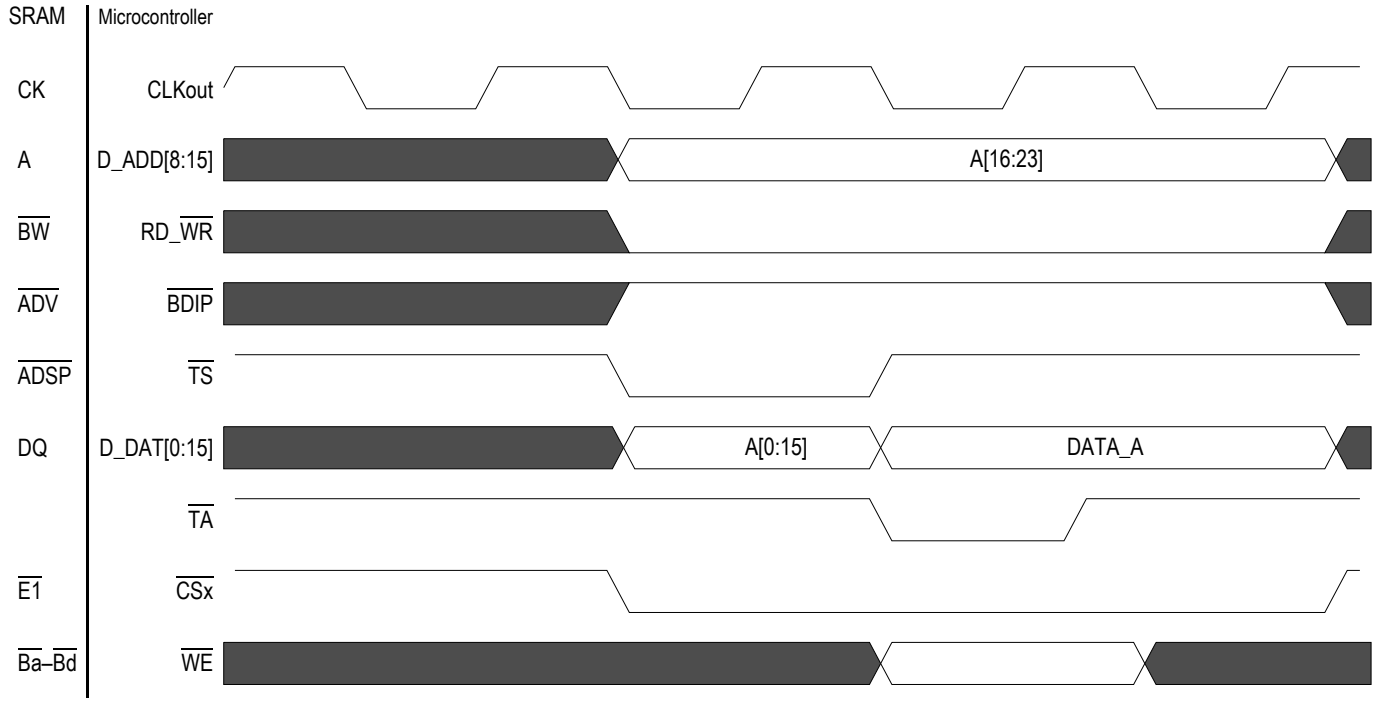


Figure 3 illustrates a flow through read, which is also referenced as a zero wait state read. When the SRAM operates in Flow Through mode, the read command is clocked in and data is referenced to the same rising edge of clock.

Figure 3: 16-bit Flow Through mode or Zero Wait State Read

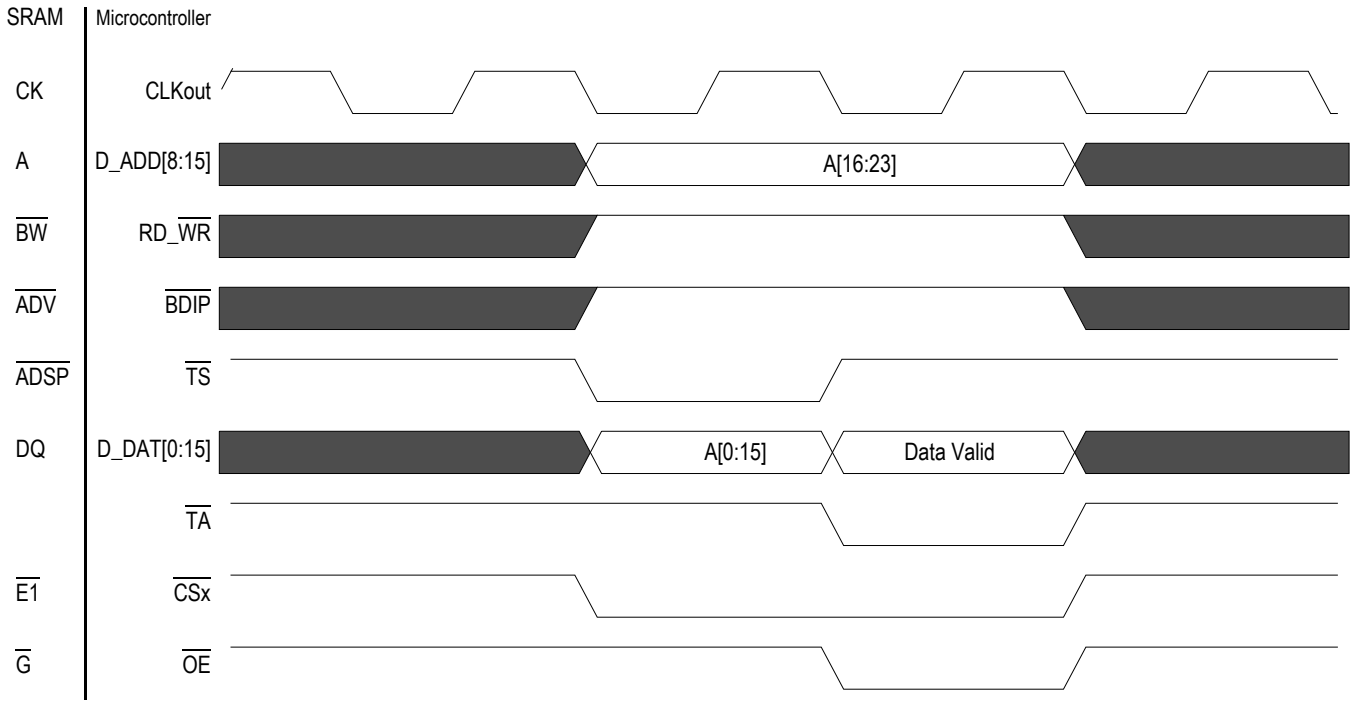


Figure 4 illustrates a flow through read cycle followed by a write cycle. One thing to notice is the required deselect cycle that is added between the read cycle and the write cycle. The deselect cycle is necessary to allow the SRAM to get off the bus and the microcontroller to begin driving. If this cycle is omitted, there will be bus contention and it is possible that the microcontroller will not latch in correct data.

Figure 4: 16-bit Flow Through Read/Write

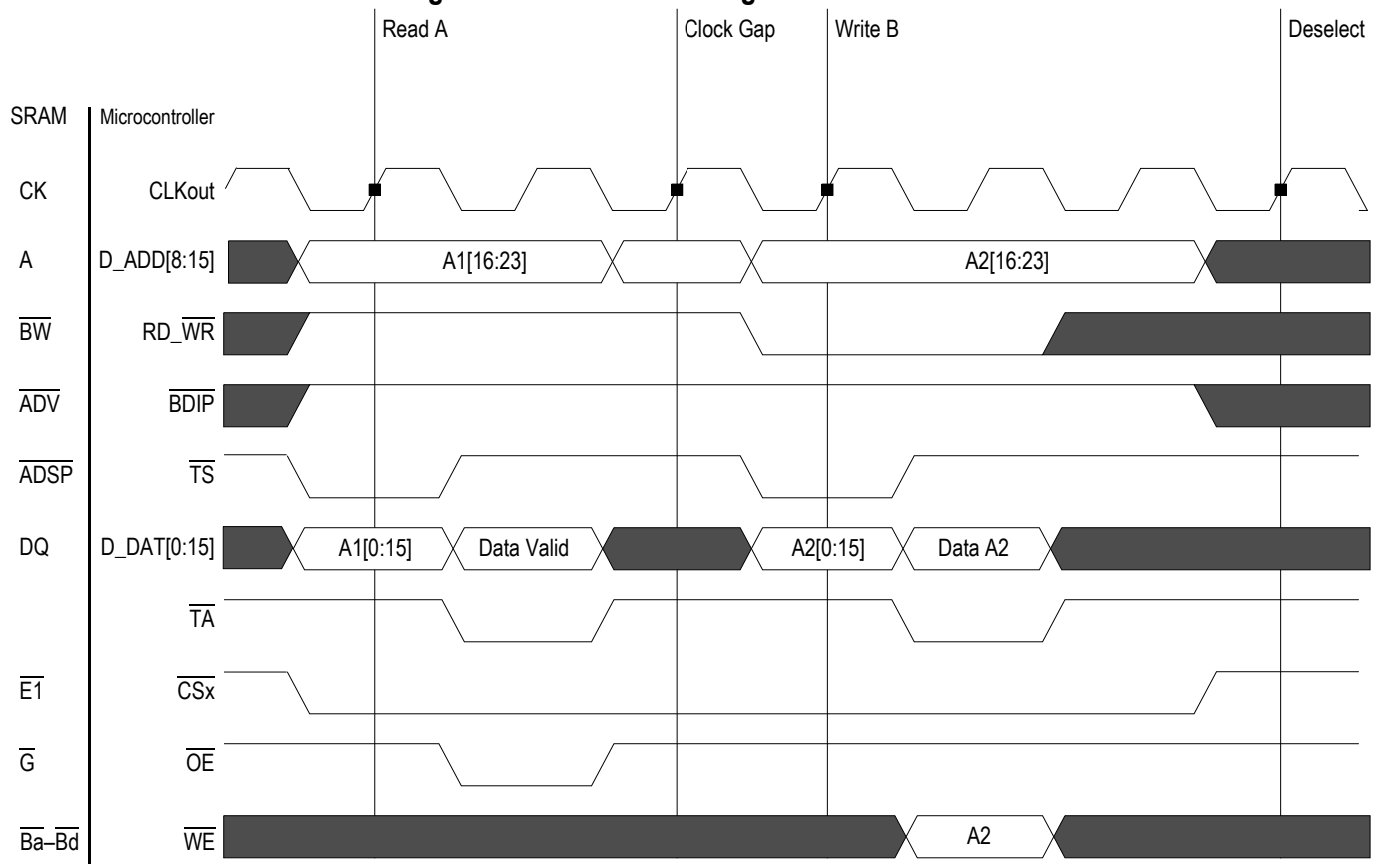
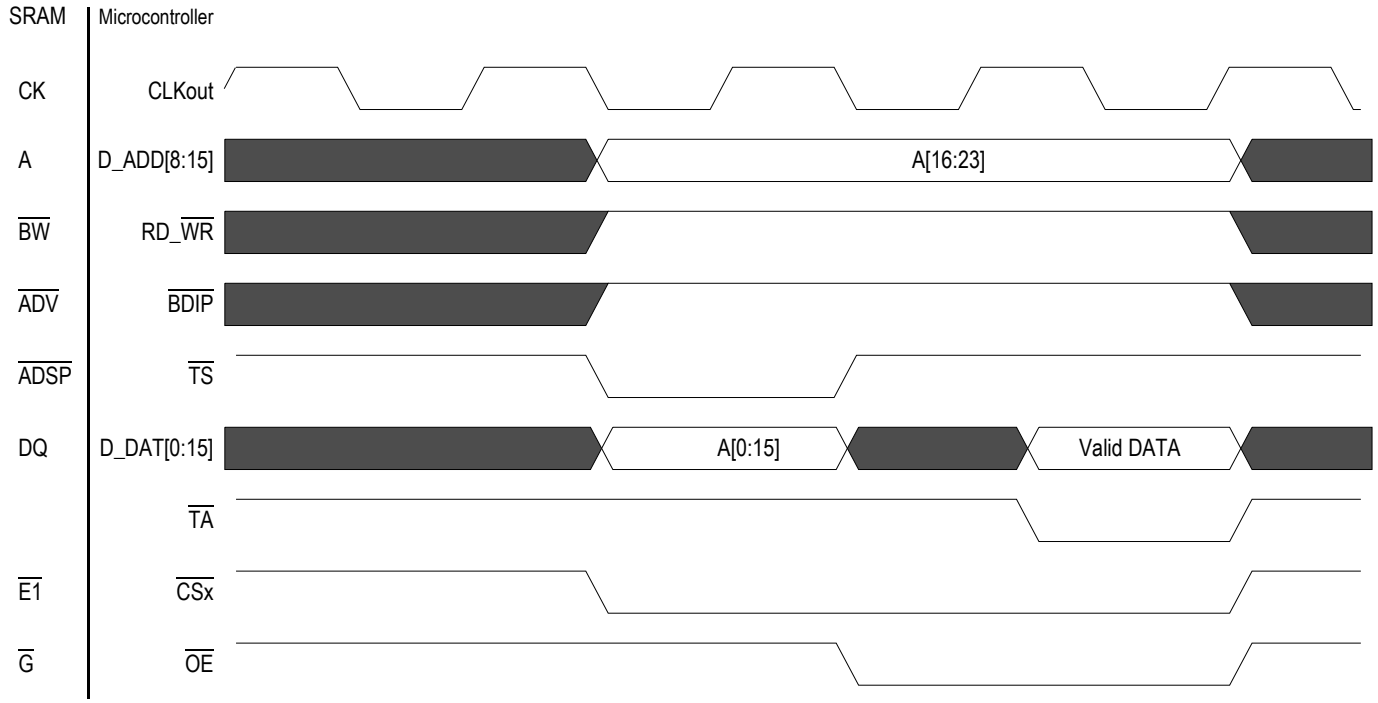


Figure 5 illustrates a pipeline read, which is also referenced as a one wait state read. The read address is supplied on the rising edge of clock. On the next rising edge of the clock, data is driven out from the SRAM. The data is referenced to the second rising edge of clock.

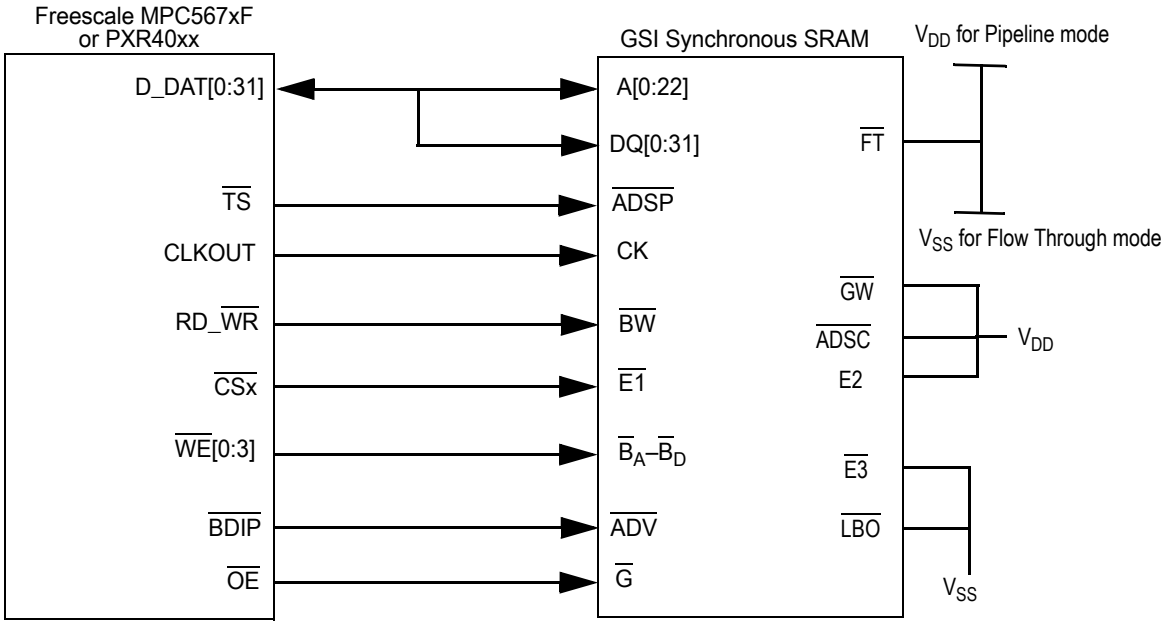
Figure 5: 16-bit Pipeline Read or One Wait State Read



Interfacing Using 32-bit Multiplexed Mode

Figure 6 shows the basic connection between either an MPC567xF or PXR40xx and a GSI SRAM. Both the MPC567xF and PXR40xx have been configured internally to interface with the SRAM using 32-bit Multiplexed mode. During an address cycle while operating in 32-bit Multiplexed mode, the microcontroller utilizes the Data Bus D_DAT[9:30] to issues addresses A[0:22]. The $\overline{FT}$ pin controls whether the SRAM operates in Pipeline mode or Flow Through mode. This pin needs to be tied to V_{SS} if the microcontroller is operating in a zero wait state Read mode, which is also referred to as Flow Through mode in the SRAM datasheet. The $\overline{FT}$ pin will need to be tied to V_{DD} if the microcontroller is operating in a one wait state Read mode, which is also referred to as Pipeline mode in the SRAM datasheet.

Figure 6: Connection diagram 32-bit Multiplexed mode



The MPC567xF and PXR40xx microcontrollers use a Late Write protocol when performing L2 cache writes. This requires the design to use the $\overline{\text{ADSP}}$ pin to configure the SRAM to utilize a Late Write protocol. For all of the following timing diagrams, the GSI pin names are displayed on the left next to the microcontroller pin names.

Figure 7 is a timing diagram for L2 cache write. As seen in **Figure 7**, the addresses, supplied on the D_DAT bus, and $\overline{\text{ADSP}}$ signals are supplied on the first rising edge of clock for the beginning of the write cycle and the write enable, byte writes, and data signals are supplied on the following rising edge of clock.

Figure 7: L2 Cache Write in 32-bit Multiplexed mode

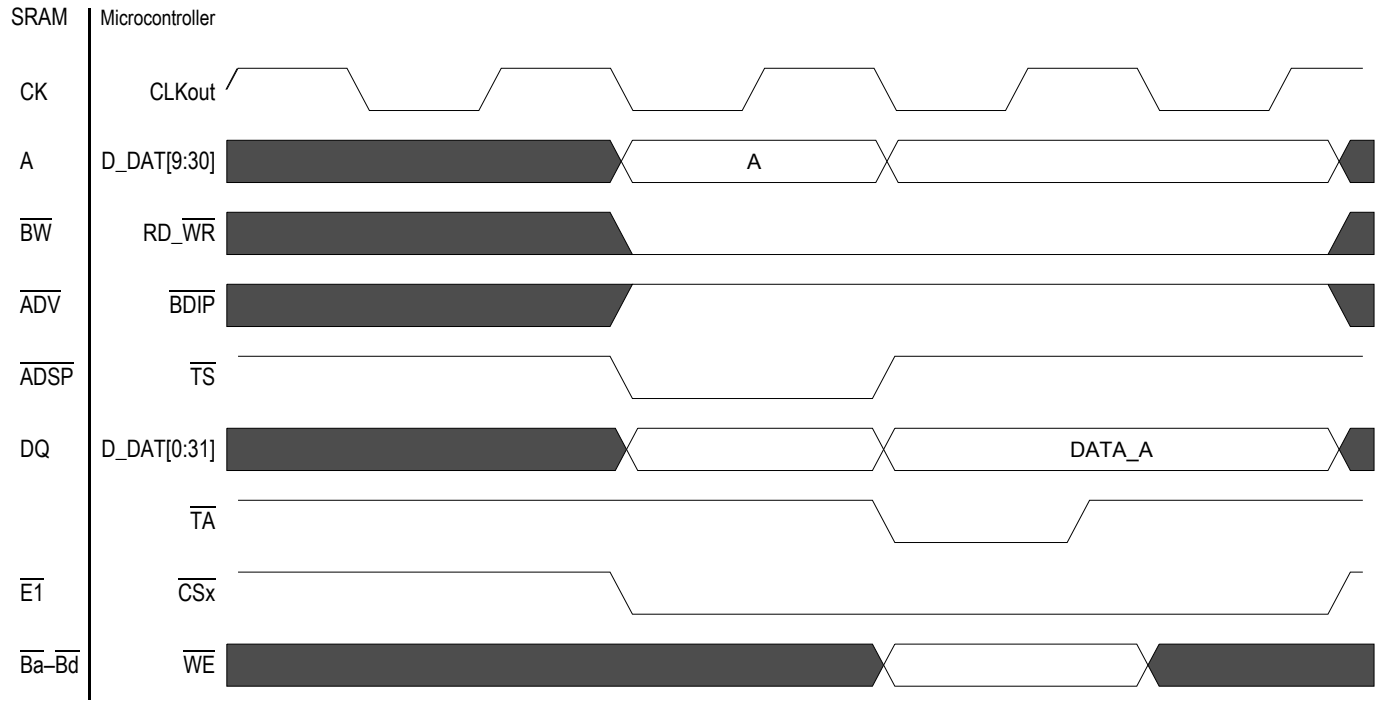


Figure 8 illustrates a flow through read, which is also referenced as a zero wait state read. When the SRAM operates in Flow Through mode, the read command is clocked in and data is referenced to the same rising edge of clock.

Figure 8: 32-bit Flow Through mode or Zero Wait State Read

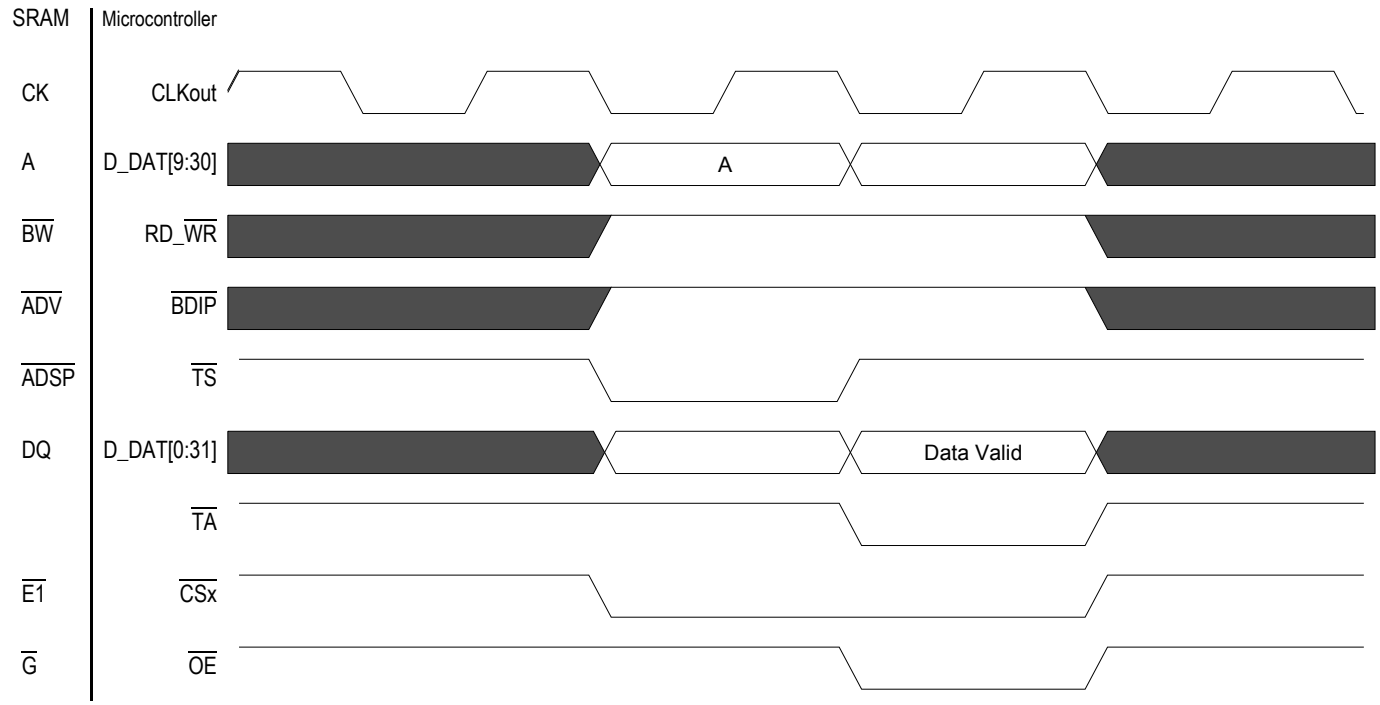


Figure 9 illustrates a flow through read cycle followed by a write cycle. One thing to notice is the required deselect cycle that is added between the read cycle and the write cycle. The deselect cycle is necessary to allow the SRAM to get off the bus and the microcontroller to begin driving. If this cycle is omitted, there will be bus contention and it is possible that the microcontroller will not latch in correct data.

Figure 9: 32-bit Flow Through Read/Write

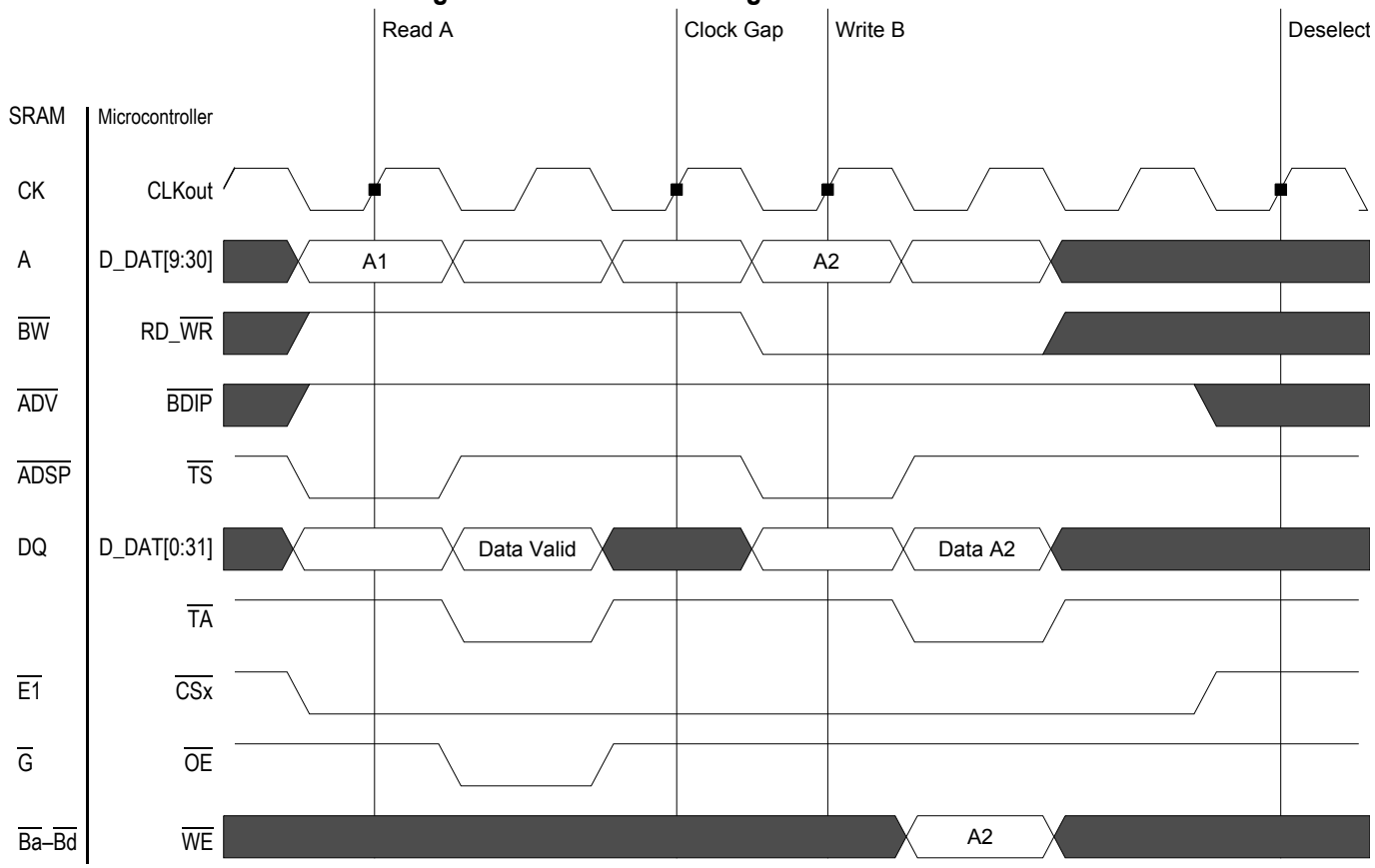
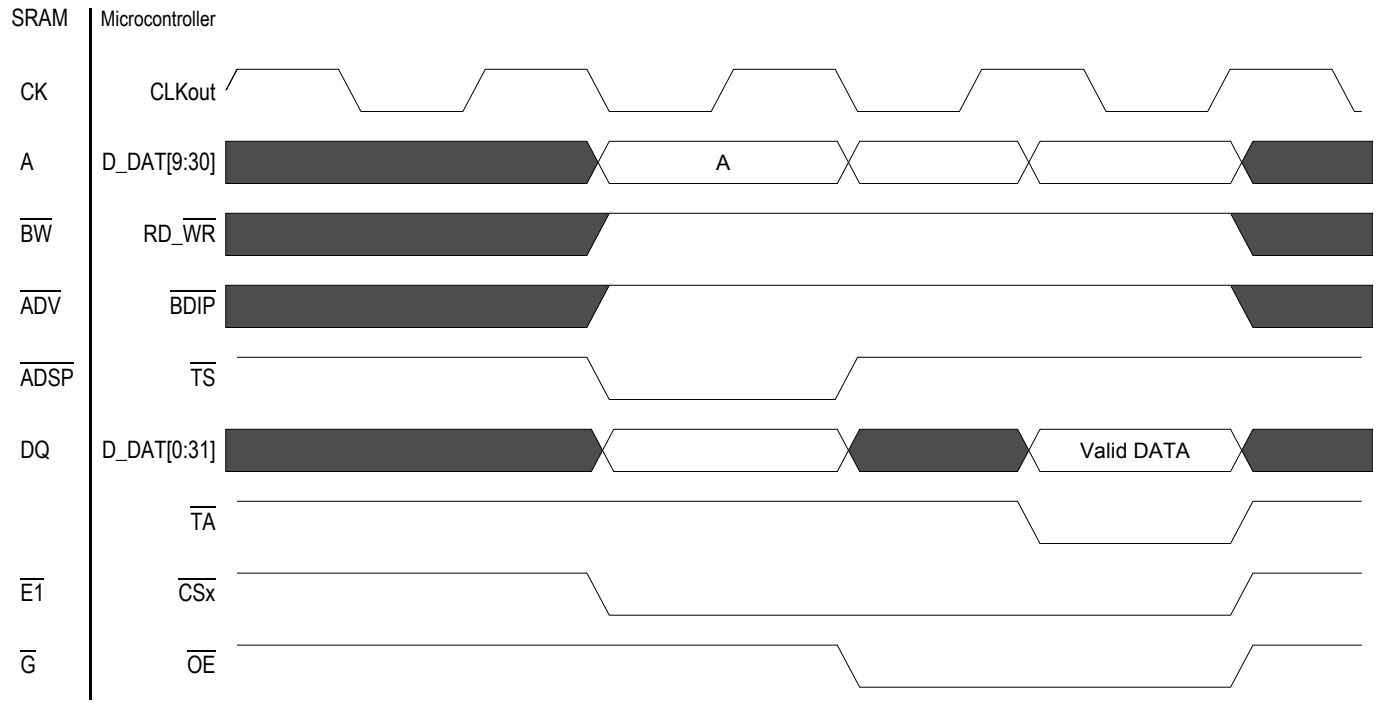


Figure 10 illustrates a pipeline read, which is also referenced as a one wait state read. The read address is supplied on the rising edge of clock. On the next rising edge of the clock, data is driven out from the SRAM. The data is referenced to the second rising edge of clock.

Figure 10: 32-bit Pipeline Read or One Wait State Read



Summary

The Freescale MPC567xF and PXR40xx microcontrollers will interface with GSI Synchronous Burst SRAMs that are configured to operate in either Pipeline or Flow Through mode. The timing diagrams in this document bridged the gap between those provided in the Freescale documentation referencing the microcontroller signal names and GSI Synchronous Burst SRAM signal names. A designer using this document as a guide should be able to properly configure the interface to work with GSI Synchronous BurstRAM devices. If further questions still exist, please feel free to contact GSI Application Engineers at apps@gsitechnology.com.

