SigmaQuad-II+ and SigmaDDR-II+ On-Die Termination (ODT)

Introduction

When an electrical signal is transmitted along a transmission line, it is reflected back when it reaches the end of the line. That reflection induces noise which adversely affects the quality of the signal, thereby making it more difficult for the receiving device to detect the state of the signal reliably. One way to resolve this issue is via termination, which reduces the reflection of transmitted signals. Termination can be implemented on the system board via external resistors. However, the benefit of termination is a function of how close it is to the end of the transmission line (i.e., the closer it is to the end of the transmission line, the less the reflection) and external resistors can only be placed so close to the receiving device. In addition, there is still transmission line through the package of the receiving device before the signal reaches the device's inputs (i.e., the very end of the transmission line).

Consequently, a better solution to this issue is "On-Die Termination", in which the termination is implemented on the die of the receiving device, directly at its inputs. Not only does this maximize the benefit of termination, but it also reduces system board cost and saves system board space (because no external resistors are needed), as well as simplifies system board signal routing.

The following GSI SigmaQuad-II+ and SigmaDDR-II+ SRAMs offer programmable On-Die Termination:

Part Number	Type	Density	ECC	Read Latency
GS8672Q37/19A	Quad B2 (SIO)	72Mb	Yes	2.0 cycles
GS8672D37/19A	Quad B4 (SIO)	72Mb	Yes	2.0 cycles
GS8672D38/20A	Quad B4 (SIO)	72Mb	Yes	2.5 cycles
GS8672T38/20A	DDR B2 (CIO)	72Mb	Yes	2.5 cycles
GS81302Q37/19/10/07	Quad B2 (SIO)	144Mb	No	2.0 cycles
GS81302D37/19/10/07	Quad B4 (SIO)	144Mb	No	2.0 cycles
GS81302T37/19/10/07	DDR B2 (CIO)	144Mb	No	2.0 cycles
GS81302D38/20/11/06	Quad B4 (SIO)	144Mb	No	2.5 cycles
GS81302T38/20/11/06	DDR B2 (CIO)	144Mb	No	2.5 cycles
GS8662Q37/19/10/07B	Quad B2 (SIO)	72Mb	No	2.0 cycles
GS8662D37/19/10/07B	Quad B4 (SIO)	72Mb	No	2.0 cycles
GS8662T37/19/10/07B	DDR B2 (CIO)	72Mb	No	2.0 cycles
GS8662D38/20/11/06B	Quad B4 (SIO)	72Mb	No	2.5 cycles
GS8662T38/20/11/06B	DDR B2 (CIO)	72Mb	No	2.5 cycles

The termination is implemented, via symmetric pull-up (to V_{DDQ}) and pull-down (to V_{SS}) transistors, on the following signals:

- Input Clocks (K, $\overline{K}$) in all devices,
- Byte Write Enables ($\overline{BW}$) in all devices,
- Input Data (D) in Quad B4 devices, and

• I/O Data (DQ) in DDR B2 devices.

Enabling/Disabling ODT

In all devices, the termination can be enabled and disabled via a dedicated "ODT" pin—pin 6R.

• When ODT = 1, termination is enabled.

• When ODT = 0, termination is disabled.

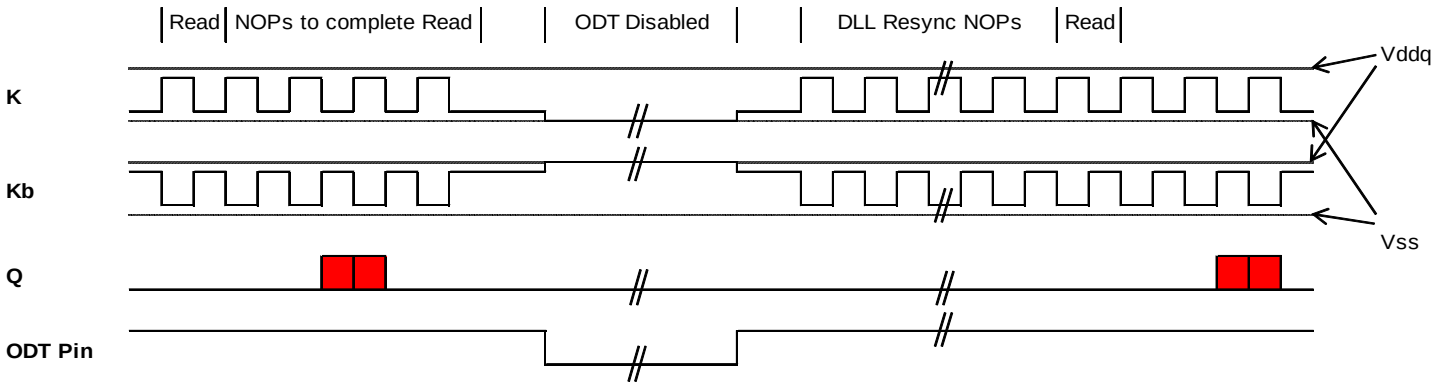
Dynamic ODT Pin Control

It is expected that most applications will simply tie the ODT pin High or Low on the system board to enable or disable termination as desired. However, the ODT pin *can* be controlled dynamically in those applications that want to enable and disable termination at various stages of system operation. For example, an application may want to enable termination during normal Read/Write operation, but disable it during extended periods of idle/inactive time in order to save power during those times. In that case, the ODT pin should be controlled in the following manner:

Step 1: Initiate several NOP operations to ensure that the last Read or Write operation completes successfully.
Step 2: Stop the input clocks.
Step 3: Change the state of the ODT pin.
Step 4: Restart the input clocks.
Step 5: Wait the appropriate number of cycles for the on-chip DLL to resynchronize before initiating new Read and Write operations.

This sequence will ensure that, when the termination is enabled and disabled dynamically, the waveforms of the input clocks are not adversely affected, and, consequently, SRAM data is not corrupted.

Timing Diagram: Read Latency = 2.5 cycles, SigmaQuad (example)



See the **Design Considerations** section below for further information on ODT operation.

Programming ODT Impedance

The termination impedance in these devices is programmed via the same RQ resistor (connected between the ZQ pin and V_{SS}) used to program output driver impedance, and is nominally RQ*0.6 Thevenin-equivalent (i.e., the individual impedances of the pull-up and pull-down transistors are nominally RQ*1.2) when RQ is between 175Ω and 250Ω. Periodic readjustment of the termination impedance occurs automatically, to compensate for drifts in supply voltage and temperature.

Accuracy

The accuracy of the termination impedance differs between the GS8672A and the GS81302 and GS8662B devices, as follows:

- In the GS8672A devices, the impedance accuracy is within ±25% of the nominal Thevenin-equivalent value of RQ*0.6.
- In the GS81302 and GS8662B devices, the impedance accuracy is within ±15% of the nominal Thevenin-equivalent value of RQ*0.6.

Design Considerations

Terminated Input Signals

When ODT = 1, the termination pull-up and pull-down transistors on uni-directional input signals (K, $\overline{K}$, and $\overline{BW}$ in all devices, and D in Quad B4 devices) are always enabled.

GSI recommends that the SRAM Controller (henceforth referred to simply as the Controller) always drive terminated inputs either High or Low. It should never leave the inputs floating, because the SRAM termination will pull floating inputs to $V_{DDQ}/2$, which (in most applications) is equal to the reference voltage V_{REF} supplied to the differential amplifiers used to receive the signals, which could cause the differential amplifiers to enter a meta-stable state and prevent the SRAM from operating within specification.

Terminated I/O Signals

When ODT = 1, the termination pull-up and pull-down transistors on bi-directional I/O signals (DQ in DDR B2 devices) are enabled and disabled according to the state of the SRAM. The enable/disable timing differs slightly between the GS8672A and GS81302 and GS8662B devices.

In GS8672A devices:

- DQ termination pull-up transistors are always enabled, except from 0.5 cycles before the SRAM begins driving Read Data onto the DQ bus, to 0.5 cycles after the SRAM stops driving Read Data onto the DQ bus.
- DQ termination pull-down transistors are always enabled, except while the SRAM is driving Read Data onto the DQ bus.

In GS81302 and GS8662B devices:

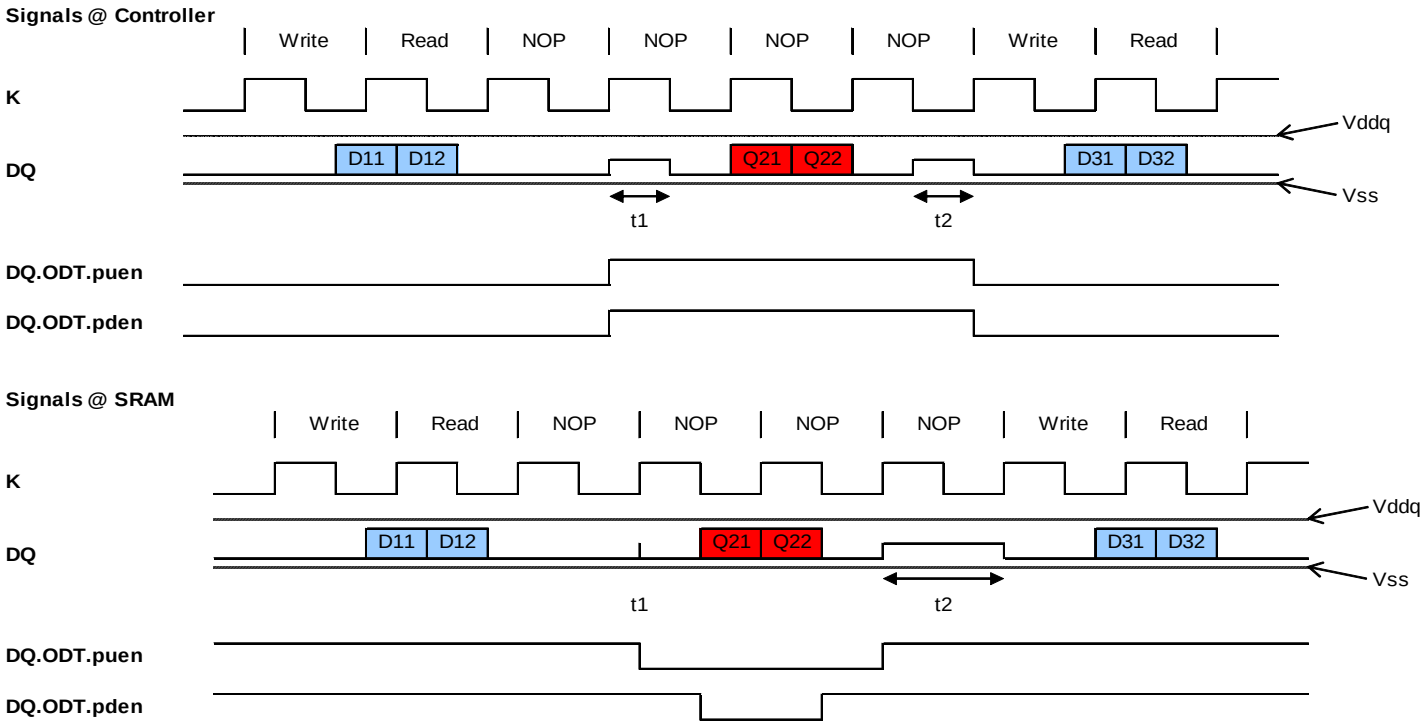
- DQ termination pull-up and pull-down transistors are always enabled, except from 0.5 cycles before the SRAM begins driving Read Data onto the DQ bus, to 0.5 cycles after the SRAM stops driving Read Data onto the DQ bus.

For all devices, GSI recommends that the Controller:

- Drive the DQs Low as described in **Note 2** in the timing diagrams below, rather than leave the DQs floating during those times, in order to prevent the SRAM termination from pulling the DQs to $V_{DDQ}/2$ during those times.
- Enable its DQ termination similar to what is described in **Note 2** in the timing diagrams below. The exact Controller DQ termination enable timing described in **Note 2** (i.e., from 0.5 cycles before the SRAM begins driving Read Data to 1.5 cycles after the SRAM stops driving Read Data) is for illustrative purposes only, to show the impact of this timing on the state of the DQs. In actuality, the Controller should minimize the amount of time it enables its DQ termination both before it begins receiving Read Data from the SRAM and after it stops receiving Read Data from the SRAM, in order to minimize the amount of time the Controller termination pulls the DQs to $V_{DDQ}/2$.

See the similar recommendation for Terminated Input Signals above for why these recommendations are important.

GS8672A Timing Diagram: Read Latency = 2.5 cycles, Transmission Delay between Controller & SRAM = 0.25 cycles



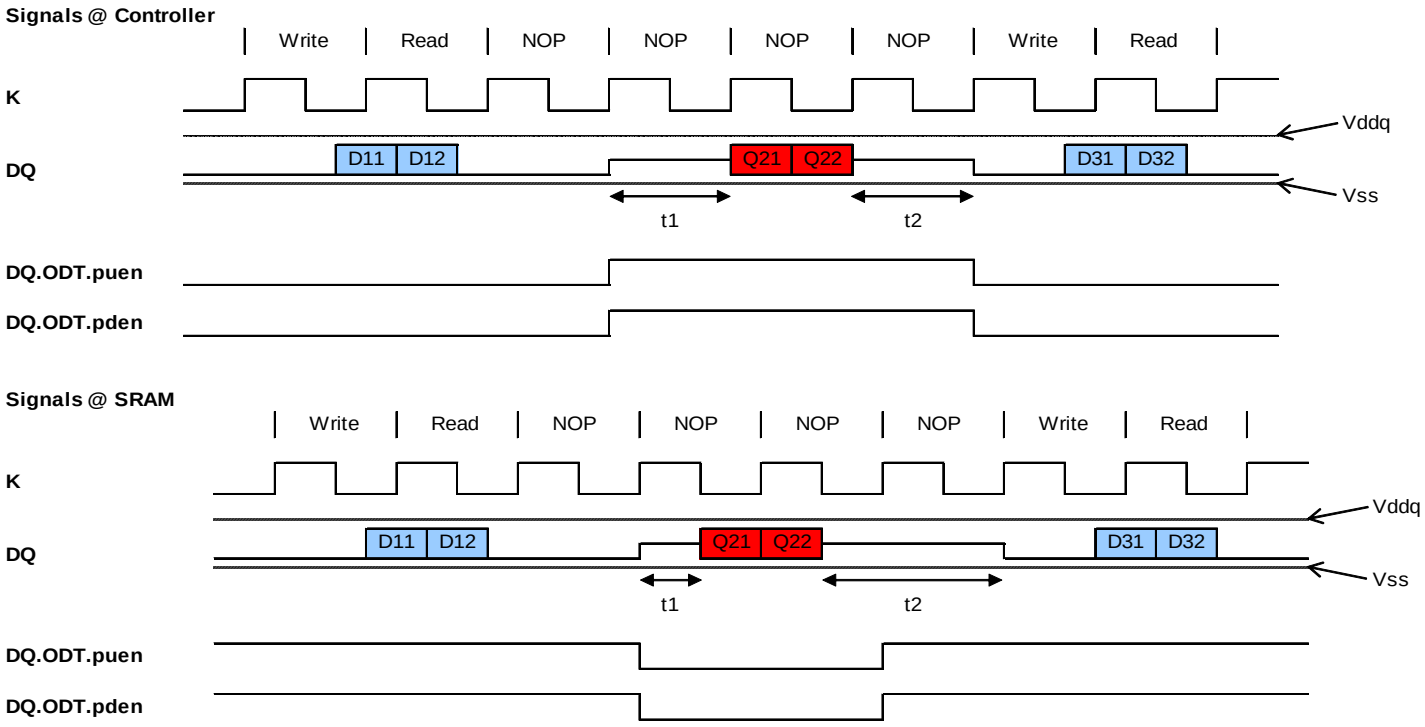
Notes:

1. "puen" indicates "pull-up transistor enable"; "pden" indicates "pull-down transistor enable".
2. The timing diagram assumes that the Controller drives DQs Low at all times, except:
   - when it is driving Write Data, and
   - from 0.5 cycles before the SRAM begins driving Read Data to 1.5 cycles after the SRAM stops driving Read Data, during which time it enables its DQ termination in order to receive that Read Data.
3. "t1" indicates the time:
   - from when the Controller stops driving DQs Low and enables its DQ ODT.pu & ODT.pd,
   - to when the SRAM disables its DQ ODT.pu.

   During "t1", the DQ bus will be pulled to $V_{DDQ}/2$, by both Controller & SRAM ODT.
   "t1" shrinks from 0.5 cycles at Controller to 0 cycles at SRAM, with this particular transmission delay.
4. "t2" indicates the time:
   - from when the SRAM enables its DQ ODT.pu,
   - to when the Controller disable its DQ ODT.pu & ODT.pd and begins driving DQs Low again.

   During "t2", the DQ bus will be pulled to $V_{DDQ}/2$, by both Controller & SRAM ODT.
   "t2" shrinks from 1 cycle at the SRAM to 0.5 cycles at the Controller, with this particular transmission delay.

GS81302 and GS8662B Timing Diagram: Read Latency = 2.5 cycles, Transmission Delay between Controller & SRAM = 0.25 cycles



Notes:

1. "puen" indicates "pull-up transistor enable"; "pden" indicates "pull-down transistor enable".
2. The timing diagram assumes that the Controller drives DQs Low at all times, except:
   - when it is driving Write Data, and
   - from 0.5 cycles before the SRAM begins driving Read Data to 1.5 cycles after the SRAM stops driving Read Data, during which time it enables its DQ termination in order to receive that Read Data.
3. "t1" indicates the time:
   - from when the Controller stops driving DQs Low and enables its DQ ODT.pu & ODT.pd,
   - to when the SRAM begins driving Read Data onto the DQ bus.

   During "t1", the DQ bus will be pulled to $V_{DDQ}/2$, first by both Controller & SRAM ODT, then by Controller ODT only.
   "t1" shrinks from 1 cycle at the Controller to 0.5 cycles at the SRAM, with this particular transmission delay.
4. "t2" indicates the time:
   - from when the SRAM stops driving Read Data onto the DQ bus,
   - to when the Controller disables its DQ ODT.pu & ODT.pd and begins driving DQs Low again.

   During "t2", the DQ bus will be pulled to $V_{DDQ}/2$, first by Controller ODT only, then by both Controller & SRAM ODT.
   "t2" shrinks from 1.5 cycles at the SRAM to 1 cycle at the Controller, with this particular transmission delay.

Note: The DQ ODT enable/disable methodology implemented in SigmaDDR-IIIe devices is electrically superior to that implemented in SigmaDDR-II+ devices. See the **SigmaDDR-IIIe DQ ODT Control application note (AN1016)** for further information.

Compatibility

Other SRAM suppliers offer II+ Quad B4 and DDR B2 devices with ODT. GSI's implementation is very similar to, but not exactly the same as, the other suppliers' implementations.

Similarities

- Other suppliers utilize an "ODT" pin at 6R in devices that support ODT, the same as GSI does in its devices.
- Other suppliers implement ODT on Input Clocks (K, $\overline{K}$), Byte Write Enables (BW), and Input Data (D, DQ), the same as GSI does on its devices.
- Other suppliers enable K, $\overline{K}$, BW, and D termination pull-up and pull-down transistors at all times, the same as GSI does on its devices.
- Other supplies enable/disable DQ termination pull-up and pull-down transistors the same as GSI does on its GS81302 & GS8662B devices.

  Although GSI GS8672A implementation differs slightly in this respect, it should be compatible with applications designed to the GSI GS1302 & GS8662B (and other suppliers') implementations.
- Other suppliers program termination impedance via the RQ resistor, the same as GSI does on its devices.
- Other suppliers' termination impedance accuracy is +/-15%, the same as in GSI's GS81302 & GS8662B devices.

Although GSI GS8672A termination impedance accuracy is somewhat worse, it should have negligible impact on signal quality. From a signal quality standpoint, driver impedance accuracy is much more important than termination impedance accuracy.

Differences

- Some suppliers only offer ODT on II+ devices with Read Latency = 2.5 cycles. Other suppliers offer ODT on II+ devices with Read Latency = 2.0 or 2.5 cycles. There is no "standard" on this particular issue.
- Other suppliers define the ODT pin differently than GSI does. Specifically, they define it as follows:

ODT = 0: enables "strong" On-Die Termination; nominal impedance is RQ*0.3 Thevenin-equivalent, for RQ between 175Ω and 350Ω. Differs from GSI definition, which uses this setting to disable On-Die Termination.

ODT = 1: enables "weak" On-Die Termination; nominal impedance is RQ*0.6 Thevenin-equivalent, for RQ between 175Ω and 250Ω. Same as GSI definition.

Note: There is no way to disable ODT in other suppliers' II+ devices that implement ODT. For now, other suppliers offer different part numbers for II+ devices without ODT. **However, some suppliers are considering offering II+ devices with an ODT pin definition identical to GSI's, in the future.**

Advantages

GSI's ODT pin definition provides the user with a couple of advantages over other suppliers' definition.

- ODT enable/disable can be dynamically controlled, in those applications that might want to do so for power-savings or other reasons.

- Simplifies inventory management in applications where multiple SRAMs are used, but ODT is only enabled on some of them.

  For example, an application may implement "depth expansion", in which two SRAMs share the same set of clock, address, and data input signals from the Controller. In that case, the application would typically only enable ODT on one of the two SRAMs, allowing one SRAM to provide the termination for both devices.

In that example, with GSI's ODT pin definition, the same device/part number can be used for both SRAM sockets. Whereas, with other suppliers' ODT pin definition, one device/part number would have to be used for the SRAM socket that enables termination, and a separate device/part number would have to be used for the SRAM socket that doesn't enable termination.

