SigmaQuad-IIIe Input Clocking Schemes

KD and $\overline{KD}$ Input Clocks

In previous industry-standard synchronous SRAMs (e.g., Burst SRAMs, NBT™ SRAMs, SigmaQuad/DDR/QDR™ -I/-II/-II+ SRAMs, etc.), all synchronous Address, Control, and Write Data inputs transmitted by the SRAM Controller (henceforth referred to simply as the "Controller") to the SRAM at a particular clock phase are latched by a common input clock. In x36 versions of these SRAMs, that can equate to approximately 60 inputs that are latched by a common input clock.

As operating (clock) frequencies increase, the ability to latch so many synchronous inputs with a common input clock becomes increasingly more difficult, because any skew (introduced by the Controller and the system board) between the slowest and fastest synchronous input, with respect to that input clock, becomes an increasingly greater percentage of the cycle time, leaving a decreasingly lower percentage of the cycle time available for input setup and hold windows. This is especially true in SigmaQuad-IIIe Burst of 2 devices, because both the Write Data and the Address inputs are Double Data Rate (DDR) (i.e., they are latched twice per clock cycle, and therefore their ideal valid windows (with zero skew) are only half a clock cycle to begin with).

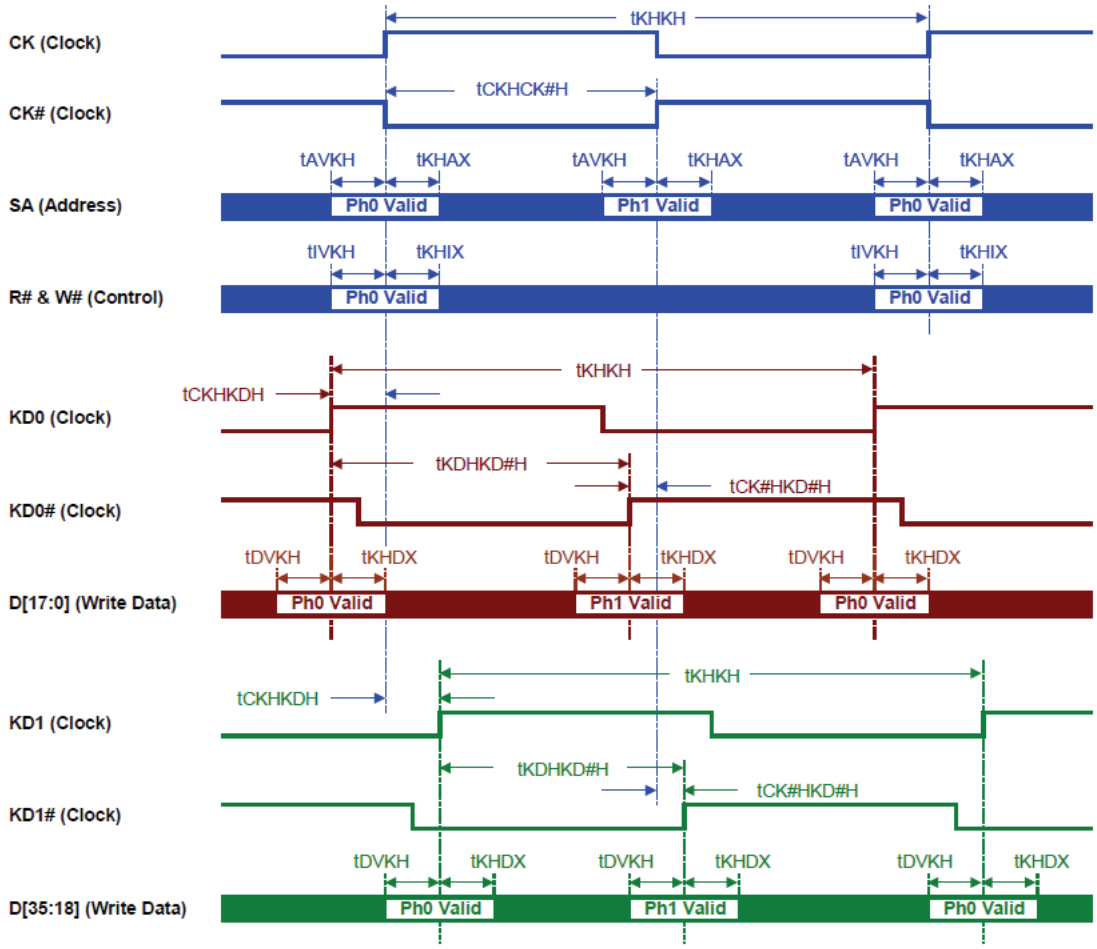
In order to address this issue, all SigmaQuad-IIIe and SigmaDDR-IIIe SRAMs have two pairs of positive and negative input clocks, KD0/$\overline{KD0}$ and KD1/$\overline{KD1}$, which are used to latch synchronous Write Data inputs only. Specifically:

- KD0 latches phase 0 DDR Write Data inputs D/DQ[17:0] in x36 devices (D/DQ[8:0] in x18 devices).
- KD1 latches phase 0 DDR Write Data inputs D/DQ[35:18] in x36 devices (D/DQ[17:9] in x18 devices).
- $\overline{KD0}$ latches phase 1 DDR Write Data inputs D/DQ[17:0] in x36 devices (D/DQ[8:0] in x18 devices).
- $\overline{KD1}$ latches phase 1 DDR Write Data inputs D/DQ[35:18] in x36 devices (D/DQ[17:9] in x18 devices).

The primary positive and negative input clocks, CK and $\overline{CK}$, are used to latch synchronous Address and Control inputs only (CK latches phase 0 Address and Control inputs; $\overline{CK}$ latches phase 1 Address inputs—no Control inputs are valid during phase 1 of the clock cycle, in SigmaQuad-IIIe devices).

By using three input clocks (CK/KD0/KD1 for phase 0 inputs, $\overline{CK}$/$\overline{KD0}$/$\overline{KD1}$ for phase 1 inputs), rather than one input clock, to latch the synchronous Address, Control, and Write Data inputs at a particular clock phase, the skew between the slowest and fastest synchronous input, with respect to the input clock used to latch them, can be reduced (the misalignment of 20 signal edges should be less than the misalignment of 60 signal edges), thereby increasing the size of the valid window and making it easier for the Controller to meet SRAM input setup and hold times.

SigmaQuad-IIIe Burst of 2 x36 Example Using KD and $\overline{KD}$ Clocks



Notes:

1. CK High to $\overline{CK}$ High timing ($t_{CKH\overline{CK}H}$) can be $t_{KHKH}/2$ ±10%.
2. KD Hight to $\overline{KD}$ High timing ($t_{KDH\overline{KD}H}$) can be $t_{KHKH}/2$ ±10%.
3. CK High to KD High timing (t_{CKHKDH}) can be ±200 ps.
4. $\overline{CK}$ High to $\overline{KD}$ High timing ($t_{\overline{CK}H\overline{KD}H}$) can be ±200 ps.

